Clock Termination Techniques and Layout Considerations

Introduction

In today's high performance systems an excellent clock source is required. The need to distribute this clock source to drive multiple devices has become more difficult as the speed and performance of application specific integrated circuits (ASICs) achieve higher limits. The higher frequencies deployed in systems cause long PCB traces to behave like transmission lines, due to the associated fast edge rates. Maintaining a balanced system requires proper termination techniques for the trace routings in the application. This application note will highlight recommended termination techniques; a comment on output loads and also presents some layout guidelines for the designer to consider.

Brief on Transmission Line Theory

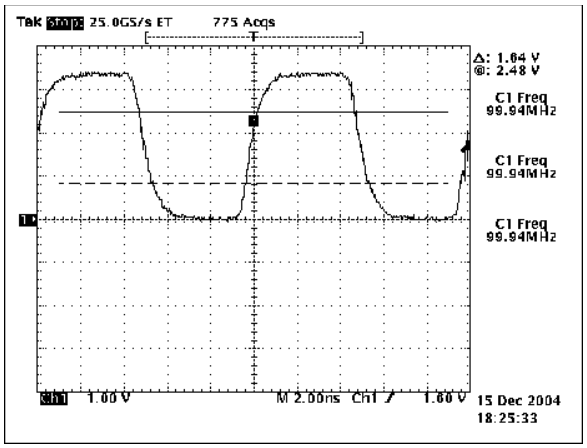
In general, most clock sources have low impedance outputs. When these devices are used to drive loads with large impedances, an impedance mismatch is present. Depending on the application conditions this impedance mismatch causes voltage reflections to occur from the load, which create steps in the clock waveform, ringing as well as overshoot and undershoot. This can result in poor system performance by degrading the clock signal at the load, false clocking of data and generating higher system noise.

In order to reduce voltage reflections a proper termination of the signal trace is necessary. The design considerations for a proper termination can be summed up in two statements:

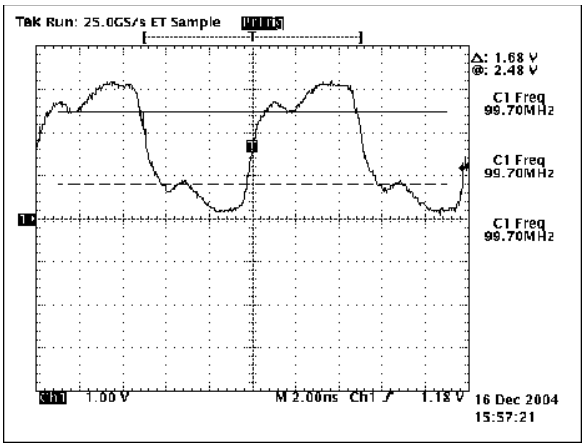
- Match the load impedance to the line impedance
- Match the source impedance to the line impedance

For most designs the first statement is the preferred method because it eliminates reflections traveling back to the clock source. This results in less noise, electromagnetic interference (EMI) and radio frequency interference (RFI).

The following illustration shows the effects of impedance mismatch on a clock source at higher frequencies.



Proper Impedance Match



Improper Impedance Match

Common Termination Techniques

As mentioned above, in order to reduce voltage reflections the trace must be properly terminated. The four basic termination techniques for a transmission line are Series, Parallel, Thevenin, and AC.

Series Termination

Series termination eliminates reflection at the clock source and helps maintain signal quality. This is best suited for TTL devices driving a small number of loads because the clock output impedance is less than the transmission line characteristic impedance. Figure 1 shows a series termination. The resistor is placed as close to the clock source as possible. Typical design values for **R** are 10Ω to 75Ω.

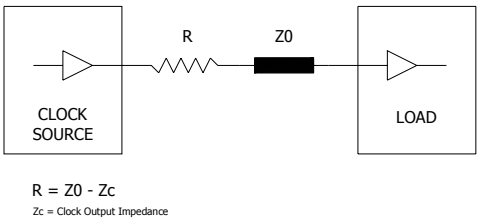


Figure 1

The value of **R** can be larger than the impedance difference in order to create a slightly over damped condition and still eliminate reflections from the clock source.

The main advantages for a Series termination are:

- Simplicity, requires only one resistor
- Power consumption is low
- Provides current limiting when driving highly capacitive loads; this can also improve jitter performance by reducing ground bounce

The major draw back for a Series termination is:

- Increases rise and fall times of the signal at the load; this may not be acceptable in some high-speed applications
- Not able to drive multiple loads

Parallel and Thevenin Terminations

The next three termination techniques provide for cleaner clock signals and eliminate reflection at the load end. These terminations should be placed as close to the load as possible.

Figure 2 depicts the Parallel termination. The Parallel termination consumes the greatest amount of power and is not recommended for low power applications. It may also change the duty cycle because the falling edge will be faster that the rising edge. It has one advantage over the Series termination in that the delay to the rise and fall time is about half.

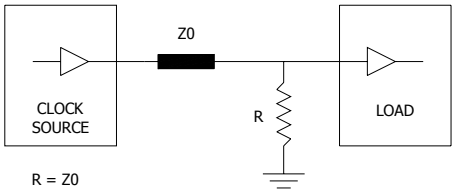


Figure 2

Thevenin termination, shown in Figure 3, will consume less power than the Parallel termination and is commonly used for PECL applications were 50Ω line matching is critical. The total value of **R** is equal to the transmission line's characteristic impedance. If an over damped condition is desired, the total value of **R** can be slightly less than the characteristic impedance. The primary drawbacks to Thevenin termination are the need for two resistors per line and the requirement for two supply voltages to be available near the termination. This termination is not recommended for TTL or CMOS circuits.

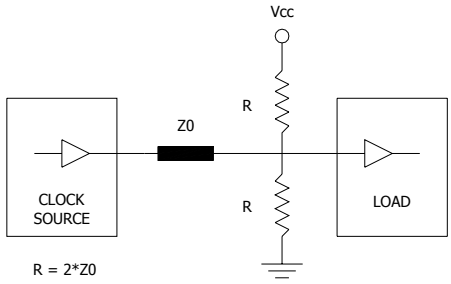


Figure 3

AC Termination

The AC termination, shown in Figure 4, adds a series capacitor in the parallel leg. The capacitor adds load to the clock source and delay due to the RC time constant, but will consume little or no power during steady state conditions. This termination is not typically recommended because it will degrade the clock signal by adding to the propagation delay time. In order to maintain an effective termination the value of $\mathbf{C_L}$ should not be less than 50pF. A larger $\mathbf{C_L}$ value will allow for rapid transition of the clock edge, but as the capacitor value increases higher current levels will pass causing an increase in power dissipation. Select an $\mathbf{R_L}$ value larger than the trace impedance to account for leakage in input impedance of the load.

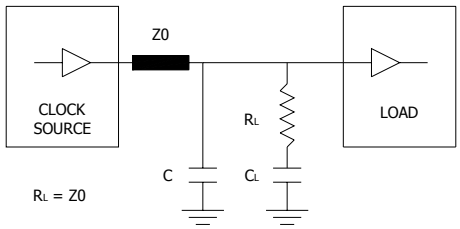
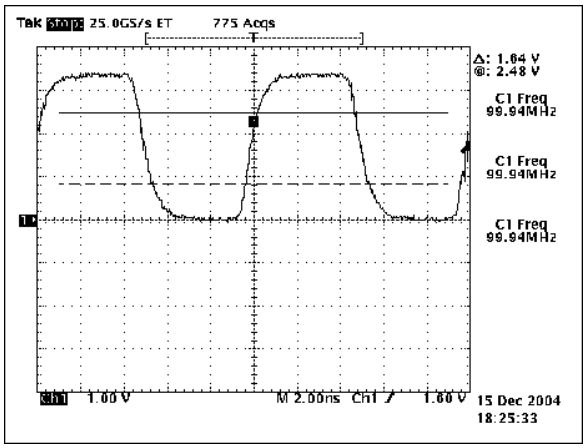


Figure 4

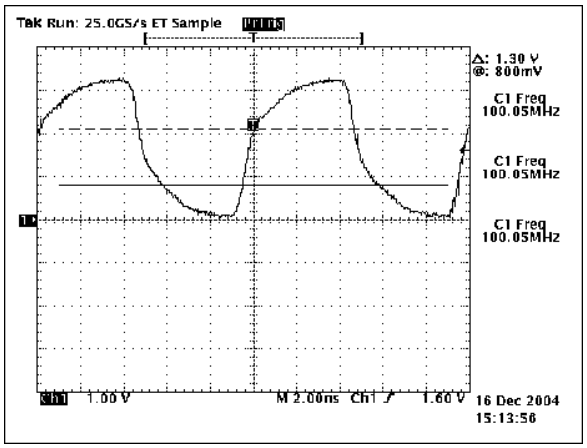
Brief on Output Loads

Care should be taken not to overload the clock source. If a single clock source is used to drive multiple loads, waveform degradation will occur if the total load exceeds the drive capability of the clock source. Some of the common symptoms of overloading are waveform clipping, symmetry imbalance, reduced signal amplitude and changes to rise and fall time values. Typically as clock frequencies increase, the capability of the source to drive higher loads will decrease. Always consult the clock source specification for maximum load capability.

The following illustration shows the effects of overloading on a clock source.



Proper Load Condition



Overload Condition

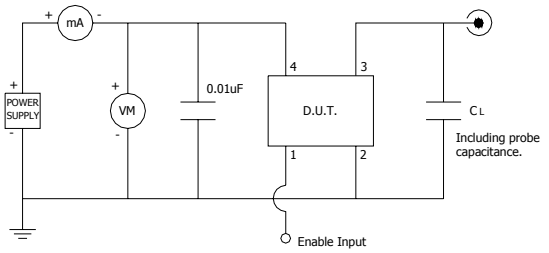
Common Clock Output Types

CTS clock oscillator designs have been developed with a variety of package options, input voltages and output types.

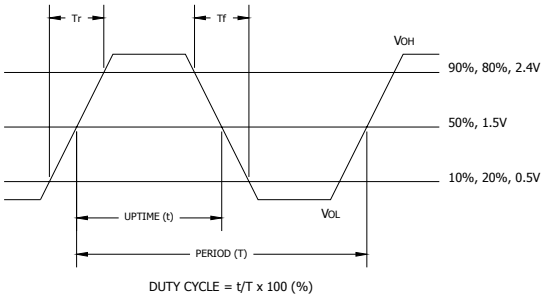
HCMOS and HCMOS/TTL Compatible

CTS designs today offer "dual compatible" oscillators, which are HCMOS output types capable of driving TTL applications. These devices inherently have greater over and under shoot due to the faster transition times. This may not be suitable for older TTL designs that have stringent EMI requirements. CTS produces two popular HCMOS/TTL compatible clock oscillators, CB3/CB3LV and Model 636.

The following illustrations show a typical HCMOS test load configuration and waveform parameters.



HCMOS Test Load



HCMOS/TTL Waveform

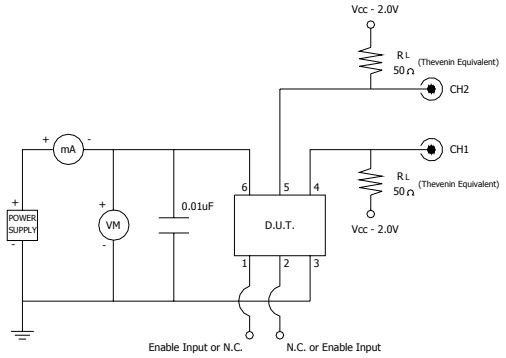
LVPECL and LVDS

CTS LVPECL and LVDS logic output designs provide many advantages over HCMOS logic technology. LVPECL and LVDS technology obtain their operating power from a positive power supply, enabling the necessary compatibility with HCMOS logic interfaces at the load points. These logic outputs also feature:

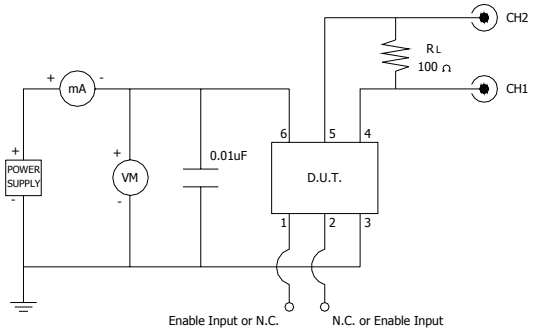
- Lower system jitter; due to smaller characteristic transition region
- Faster rise and fall times
- Offers differential outputs; essential for reducing emissions
- Ability to drive 50Ω transmission lines directly
- Lower power supply consumption at high frequencies

CTS Model 635 offers the option for either output type.

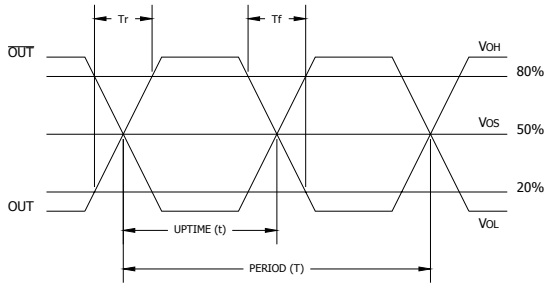
The following illustration shows a typical LVPECL and LVDS test load configuration and waveform parameters.



LVPECL Test Load



LVDS Test Load



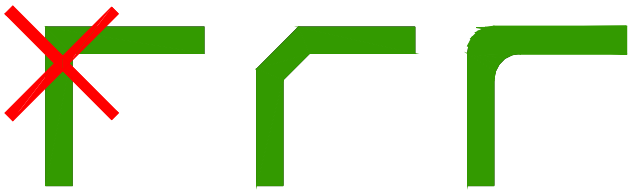
LVPECL/LVDS Waveform

Layout Guidelines

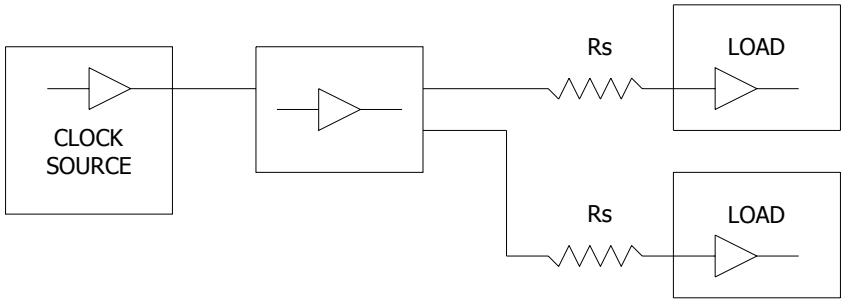
Employing good design practices during the printed circuit board layout process will minimize the signal degradations previously discussed. Some common guidelines for PCB designs are:

- Physically locate the clock source as close to the load as possible
- Limit trace lengths for clock signals
- Do not route clock signals close to the board edge
- Try to avoid using vias in clock signal routings. Vias change the trace impedance causing reflection.
- Do not route signal traces on the power and ground layer

- Avoid right angle bends in a trace and if possible keep trace routings straight. If a bend is necessary make it with two 45° corners or by using round bend (best).



- Decoupling capacitors between V_{CC} and ground of the clock source are essential to reduce noise that may be transmitted to the clock signal. These capacitors must be places as close to the V_{CC} pin as possible.
- To avoid cross talk maintain proper spacing between multiple clock sources and high-speed switching busses.
- Differential trace routings should be as close as possible to get a high coupling factor. The routings should be equal in length to avoid impedance mismatches leading to different propagation delay times.
- When driving multiple loads with a single clock source, consider splitting the routings. Make the individual routing lengths as equal as possible.



Conclusion

This application note presented an introduction to proper termination techniques for applications using clock sources that drive various loads. It also outlined layout considerations to produce a solid application design. All these techniques strive to minimize conditions that degrade clock signals that result in poor system performance.

CTS Clock Oscillator Models

The table below lists the clock oscillator products available from CTS. Use the following web link to find the latest product offerings, detailed data sheets and RoHS information for each product. http://www.ctscorp.com/components/xo.asp.

MODEL NAME	DESCRIPTION	FREQUENCY RANGE (MHz)	STABILITY	OUTPUT LOGIC	TEMPERATURE RANGE	SUPPLY VOLTAGE	PACKAGE SIZE
nWave CP5 and CP7	Programmable Clock Oscillator	2.0 - 200	± 50 ppm	HCMOS/TTL	-20 to 70°C or -40°C to 85°C	2.5V ± 10% 3.3V ± 10%	5.0 x 3.2 x 1.2 mm 0.197 x 0.126 x 0.047 inch or 7.0 x 5.0 x 1.8 mm 0.276 x 0.197 x 0.071 inch
Model 636	SMT General Purpose Clock Oscillator	1.0 - 125	± 100 ppm ± 50 ppm ± 25 ppm ± 20 ppm	HCMOS/TTL	-20 to 70°C or -40°C to 85°C	1.8V ± 10% 2.5V ± 10% 3.3V ± 10% 5V ± 10%	5.0 x 3.2 x 1.2 mm 0.197 x 0.126 x 0.047 inch
CB3 CB3LV	SMT General Purpose Clock Oscillator	1.5 - 160	± 100 ppm ± 50 ppm ± 25 ppm ± 20 ppm	HCMOS/TTL	-20 to 70°C or -40°C to 85°C	3.3V ± 10% 5V ± 10%	7.5 x 5.0 x 1.8 mm 0.295 x 0.197 x 0.071 inch
CB3-S4 CB3LV-S4	SMT Stratum 4 Clock Oscillator	1.5 - 80	± 32 ppm (Stratum 4)	HCMOS/TTL	-20 to 70°C or -40°C to 85°C	3.3V ± 10% 5V ± 10%	7.5 x 5.0 x 1.8 mm 0.295 x 0.197 x 0.071 inch
CB1V8	SMT General Purpose Clock Oscillator	1.0 - 70	± 100 ppm ± 50 ppm ± 25 ppm ± 20 ppm	HCMOS/TTL	-20 to 70°C or -40°C to 85°C	1.8V ± 10%	7.0 x 5.0 x 1.8 mm 0.276 x 0.197 x 0.071 inch
CB2V5	SMT General Purpose Clock Oscillator	1.0 - 125	± 100 ppm ± 50 ppm ± 25 ppm ± 20 ppm	HCMOS/TTL	-20 to 70°C or -40°C to 85°C	2.5V ± 10%	7.0 x 5.0 x 1.8 mm 0.276 x 0.197 x 0.071 inch
Model 635	SMT High Frequency Fundamental Clock Oscillator	19.44 - 250	± 100 ppm ± 50 ppm ± 25 ppm	LVPECL LVDS	0 to 70°C or -40°C to 85°C	3.3V ± 5% 2.5V ± 5%	7.0 x 5.0 x 2.0 mm 0.197 x 0.276 x 0.079 inch
Model 658	SMT High Frequency Multiplier Clock Oscillator	38 - 750	± 100 ppm ± 50 ppm ± 25 ppm	HCMOS LVPECL LVDS	0 to 70°C or -40°C to 85°C	3.3V ± 5% 2.5V ± 5%	7.0 x 5.0 x 2.0 mm 0.197 x 0.276 x 0.079 inch
MXO45HS MXO45HST	TH General Purpose Clock Oscillator	1 - 105	± 100 ppm ± 50 ppm ± 25 ppm ± 20 ppm	HCMOS/TTL	-20 to 70°C or -40°C to 85°C	5V ± 10%	13.0 x 13.0 x 5.1 mm 0.510 x 0.510 x 0.200 inch
MXO45 MXO45T	TH General Purpose Clock Oscillator	1 - 105	± 100 ppm ± 50 ppm ± 25 ppm ± 20 ppm	HCMOS/TTL	-20 to 70°C or -40°C to 85°C	5V ± 10%	13.0 x 20.6 x 5.1 mm 0.510 x 0.810 x 0.200 inch
MXO45HSLV MXO45HSTLV	TH General Purpose Clock Oscillator	1.5 - 50	± 100 ppm ± 50 ppm ± 25 ppm ± 20 ppm	HCMOS/TTL	-20 to 70°C or -40°C to 85°C	3.3V ± 10%	13.0 x 13.0 x 5.1 mm 0.510 x 0.810 x 0.200 inch
MXO45LV MXO45TLV	TH General Purpose Clock Oscillator	1.5 - 50	± 100 ppm ± 50 ppm ± 25 ppm ± 20 ppm	HCMOS/TTL	-20 to 70°C or -40°C to 85°C	3.3V ± 10%	13.0 x 13.0 x 5.1 mm 0.510 x 0.810 x 0.200 inch
Model 632 **Q3 2007**	SMT General Purpose Clock Oscillator	1.0 - 100	± 50 ppm ± 25 ppm	HCMOS/TTL	-20 to 70°C or -40°C to 85°C	1.8V ± 10% 2.5V ± 10% 3.3V ± 10%	3.2 x 2.5 x 1.2 mm 0.126 x 0.098 x 0.047 inch

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