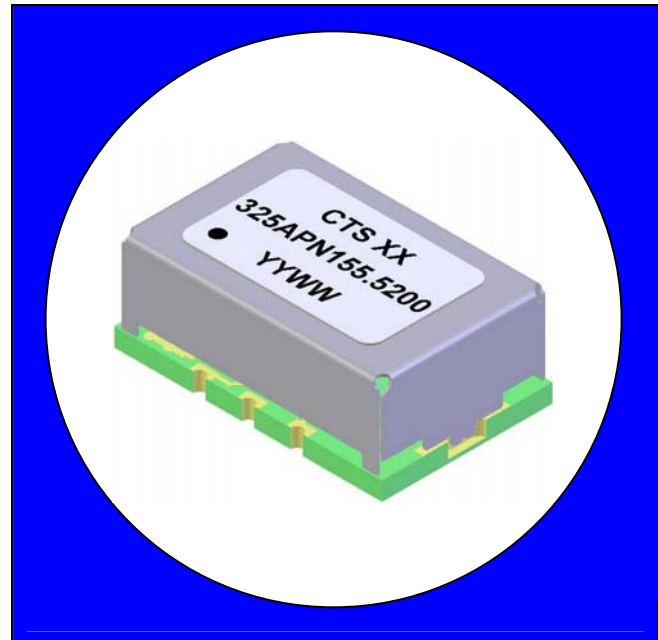


APPLICATIONS

SONET/SDH
 Clock and Data Recovery
 Frequency Translation
 Base Stations/Picocells
 Test Equipment

FEATURES

- Industry Standard 9x14mm SMT Footprint
- Output Frequencies from 15 MHz to 160 MHz
- +3.3 or 5.0 Vdc Supply Voltage Option
- -40°C to +85°C Temperature Range
- HCMOS, PECL, LVPECL, or LVDS output
- ± 10 ppm Absolute Pull Range (APR)
- Low Phase Noise
- Tape & Reel Packaging
- Fully Compliant to RoHS Directive 2002/95/EC



DESCRIPTION

The CTS Model 325 VCXO platform is a versatile , small size, high performance SMT VCXO. The high quality CTS Quartz Crystal used in this VCXO offers very low phase noise and low jitter, making it the ideal choice for any telecommunications system.

ELECTRICAL SPECIFICATIONS

Parameter	Conditions & Remarks	Min	Typical	Max	Unit
Operating Conditions					
Output Frequency Range	f_{NOM}	15	19.2, 52, 61.44,100 122.88,125 155.52	160	MHz
Operating Temperature Range	T_O	-40	-	85	°C
Storage Temperature Range	T_S	-55	-	125	°C
Maximum Supply Voltage Range	V_{CC}	-0.5	-	7.0	Vdc
Operating Supply Voltage (V_{CC})	5.0V, ±5% Option B	4.75	5.0	5.25	Vdc
	3.3V, ±5% Option A	3.135	3.3	3.465	
Supply Current (I_{CC}); $V_{CC}=5.0V$	$V_{CC} = 5.0$ Vdc ; HCMOS output	-	15	25	mA
	$V_{CC} = 5.0$ Vdc ; PECL output	-	70	85	
Supply Current (I_{CC}); $V_{CC}=3.3V$	$V_{CC} = 3.3$ Vdc ; LVCMOS output	-	15	25	mA
	$V_{CC} = 3.3$ Vdc ; LVPECL output	-	60	75	
	$V_{CC} = 3.3$ Vdc ; LVDS output	-	45	60	
Load	HCMOS / LVCMOS	$C_L = 15$ pF			
	PECL / LVPECL	50Ω to $V_{CC} - 2V$, or equivalent			
	LVDS	100Ω (differential)			

ELECTRICAL SPECIFICATIONS (continued)

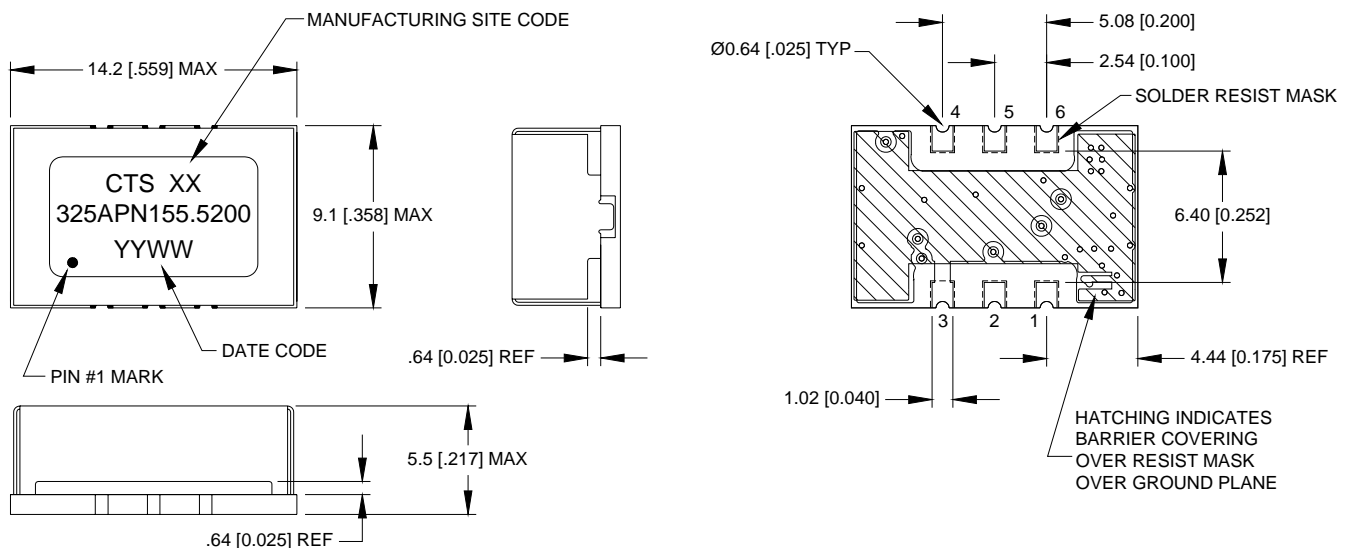
Parameter	Conditions & Remarks	Min	Typical	Max	Unit	
Frequency Stability						
Calibration	$\Delta f/f_{NOM}$; $T_A = 25^\circ\text{C}$; $V_C = 0.5 \times V_{DC}$ $V_{CC} = \text{nominal}$; at time of shipment	-	± 10	± 20	ppm	
Frequency vs. Temperature	ref to $T_A = 25^\circ\text{C}$; $V_C = \text{constant}$	-	± 15	± 25	ppm	
Frequency vs. Voltage	$V_{CC} = V_{CC} \pm 5\%$; $V_C = \text{constant}$	-	± 1	± 2	ppm	
Frequency vs. Load	$\pm 10\%$ load variation; $V_C = \text{constant}$	-	± 1	± 2	ppm	
Frequency vs. Time (Aging)	15 years	-	± 8	± 20	ppm	
Electronic Frequency Control						
Input Impedance	Z_i	100	500	-	k Ω	
Control Voltage Range	V_C ; positive monotonic transfer	0	-	V_{CC}	Vdc	
Pullability	$T_A = 25^\circ\text{C}$; ref. to $V_C = 0.5 \times V_{CC}$ $V_C = 0\text{V to } V_{CC}$	± 50	± 75	-	ppm	
Absolute Pull Range	APR; all causes (see note 1) $V_C = 0 \text{ to } V_{CC}$	± 10	± 50	-	ppm	
Bandwidth	-3dB; $V_C = 0.5 * V_{CC}$	10	-	-	kHz	
Linearity	Deviation from best linear fit	-	± 5	± 10	%	
Output Parameters						
Output Level: HCMOS/LVCMOS Option C (Maximum frequency = 125 MHz)	V_{OL} $C_L = 15\text{pF}$	-	-	$0.1 \times V_{CC}$	V	
	V_{OH} $C_L = 15\text{pF}$	$0.9 \times V_{CC}$	-	-		
Output Level: PECL/LVPECL Option P	V_{OL}			$V_{CC} - 1.62$	V	
	V_{OH}	$V_{CC} - 1.025$	-	-		
Output Level: LVDS Option L	Differential Output Swing; $R_L = 100\Omega$	247	350	454	mV	
Rise/Fall Times (20% - 80%)	PECL/LVPECL/LVDS	-	0.300	0.450	ns	
	HCMOS/LVCMOS ; $C_L = 15\text{pF}$	-	3	5		
Duty Cycle	@ 50% waveform level	40	50	60	%	
Start up time	V_{CC} @ nominal, $V_C = 0 \text{ to } V_{CC}$; $T_O = -40^\circ\text{C to } 85^\circ\text{C}$ to reach 90% of final amplitude	-	15	50	ms	
Spurious		-	-	-100	dBc	
Non and Sub-Harmonics		-	-	-100	dBc	
Phase Jitter; 155.52 MHz	12 KHz – 20 MHz bandwidth	-	0.4	1	ps	
Phase Noise: HCMOS/LVCMOS	Typical, 122.88 MHz	offset = 10Hz	-	-65	-	dBc/Hz
		100Hz	-	-95	-	dBc/Hz
		1kHz	-	-125	-	dBc/Hz
		10kHz	-	-145	-	dBc/Hz
		100kHz	-	-158	-	dBc/Hz
Phase Noise: PECL/LVPECL	Typical, 155.52 MHz	offset = 10Hz	-	-60	-	dBc/Hz
		100Hz	-	-90	-	dBc/Hz
		1kHz	-	-120	-	dBc/Hz
		10kHz	-	-142	-	dBc/Hz
		100kHz	-	-152	-	dBc/Hz

Phase Noise: LVDS	Typical @125 MHz	offset = 10Hz	-	-65	-	dBc/Hz
		100Hz	-	-95	-	dBc/Hz
		1kHz	-	-125	-	dBc/Hz
		10kHz	-	-140	-	dBc/Hz
		100kHz	-	-145	-	dBc/Hz
Output Disable (Option E)	Outputs Disabled with Pad 2 @ Logic "1"					
Output Enable	Outputs Enabled with Pad 2 @ Logic "0" or floating					

NOTE 1: Minimum guaranteed frequency shift ($\Delta f/f_{NOM}$) under all conditions (inc. temperature, aging, supply voltage, load) for 15 years

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



ALL DIMENSIONS ARE IN MM [INCHES].

ALL DIMENSIONS ARE NOMINAL UNLESS OTHERWISE SPECIFIED.

Co-Planarity (from seating plane): 0.1 [.004] MAX

Lead Termination Finish: Gold Flash, <10 micro inch, over Ni plated Cu.

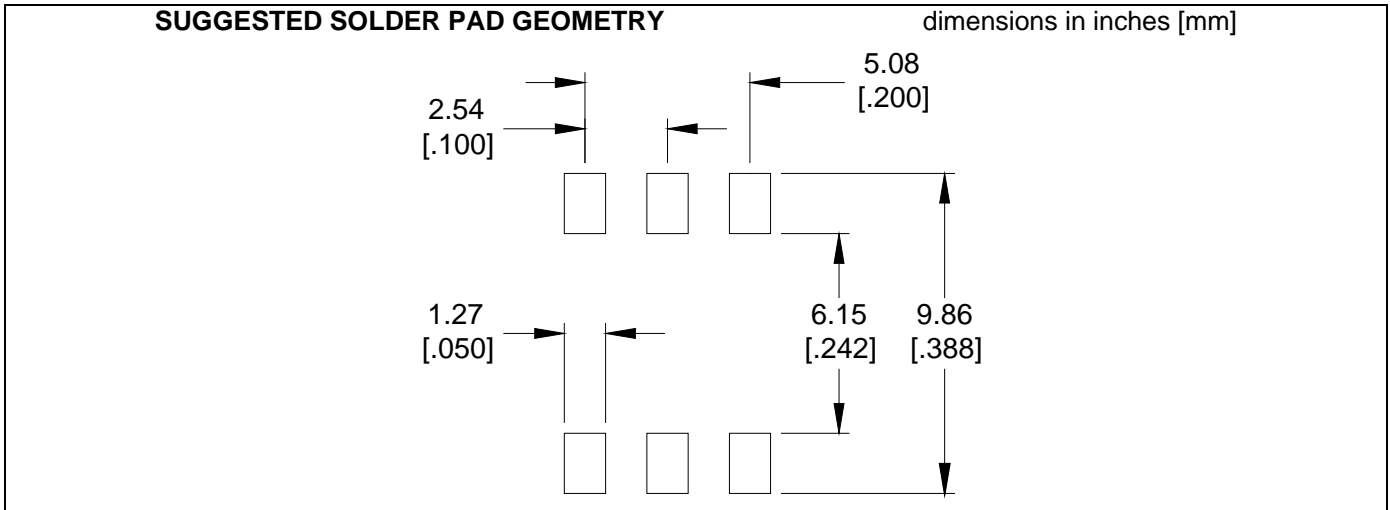
MARKING INFORMATION

CTS XX - Manufacturing Site Code.
 CTS Part Number
 (Frequency marked with 4 significant digits after decimal point)
 YYWW - Date code, YY - year, WW - week.

PIN ASSIGNMENT

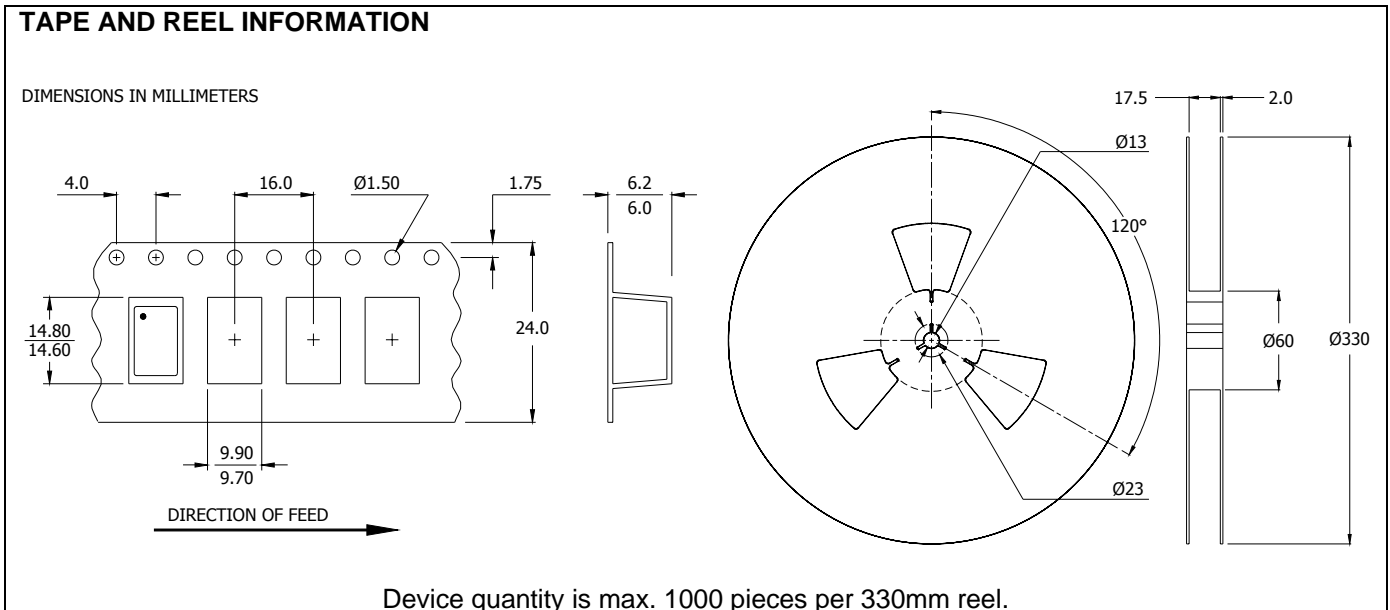
- | | |
|-------------------------|-------------------------------------|
| 1. Vc - Control Voltage | 4. RF Output |
| 2. Enable/Disable or NC | 5. Complimentary Output or NC |
| 3. Ground | 6. V _{CC} - Supply Voltage |

MECHANICAL SPECIFICATIONS (continued)



MAXIMUM SOLDERING PROFILE		
Temperature	>217°C	260°C maximum
Time	2.5 minutes maximum	10 seconds maximum

Note: Part is not designed to be reflowed in an inverted position.



ENVIRONMENTAL SPECIFICATIONS

- RoHS : Lead-Free and fully compliant to RoHS Directive 2002/95/EC
- Temperature Cycle : 400 cycles from -55°C to +125°C, 10 minute dwell at each temperature, 1 minute transfer time between temperatures.
- Mechanical Shock : 1,000g's, 0.3mS duration, 1/2 sinewave, 3 shocks each direction along 3 mutually perpendicular planes (18 total shocks).
- Sinusoidal Vibration : 0.06 inches double amplitude, 10 to 55 Hz and 10g's, 55 to 2,000 Hz, 3 cycles each in 3 mutually perpendicular planes (9 times total).
- Resistance to Solder Heat : 3 reflows of +260°C peak, 10 seconds maximum.
- High Temperature Operating Bias : 2,000 hours at +125°C, maximum bias, disregarding frequency shift.
- Frequency Aging : 1,000 hours at +85°C, full bias, less than ±3 ppm shift typical.
- Moisture Sensitivity : Level 1

Model 325 Standard Options:

