Jitter and Phase Noise in Timing References

White Paper

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JITTER & PHASE NOISE IN TIMING REFERENCES

The demand for instant data access is increasing exponentially through the development of very high data rate applications like 5G networks, IoT and IIoT communication links, cloud file management, video streaming, and continued expansion of internet usage. The Internet has become an essential communication tool in our daily life, when it comes to accessing various types of information. Users today expect to upload and download high-density data in real-time with minimal propagation delays. These trends are increasing the need for higher speeds, wider bandwidths, higher data rates, and faster data interfaces all while minimizing errors and driving latency to zero.

As communication speeds increase, system timing requirements need clock oscillators and other timing components with better noise performance. Jitter and other noise components of the reference clock have a direct impact on the efficiency of the data transferred between devices. Higher jitter from the timing source translates to high noise levels in the system and in most cases potential loss of data. The improvement in jitter performance helps boost data transfer and system efficiency.

Noise is any unwanted information from internal or external sources within a signal. Some are unavoidable while others can be removed from the system. Unwanted noise can degrade system performance and at times disrupt its operation altogether. Understanding clock jitter in applications is critical because it plays a key role in the timing budget for a given system.

The impact of oscillator noise to signals within a timing system will have the following affects:

- Limit the ability to determine the current state and the predictability of oscillators
- Limit syntonization and synchronization accuracy
- Limit receivers' useful dynamic range, channel spacing, and selectivity - can limit jamming resistance
- Limit number of subscribers within a given communication system, as noise within the transceiver operates at lower efficiency
- Limits navigation accuracy
- Limits ability to lock to narrow-line width resonances
- Cause timing errors [$\sim\tau\sigma_y(\tau)$]
- Cause bit errors in digital communication systems
- Cause loss of lock and limit acquisition/reacquisition capability in phase-locked loop

This white paper provides an overview of jitter and phase noise in crystal oscillators, which are commonly used as system timing references. CTS products that provide solutions for frequency references with low noise performance will be introduced at the end.

JITTER AND PHASE NOISE

Jitter and Phase Noise are two measures that define a given oscillator's noise figure. Jitter is the measurement of the stability in the time domain, where Phase Noise describes the short-term noise in the frequency domain.

Time vs. Frequency Domain

Figures 1a and 1b show measurements of an ideal and a real signal in the Time and Frequency domains.

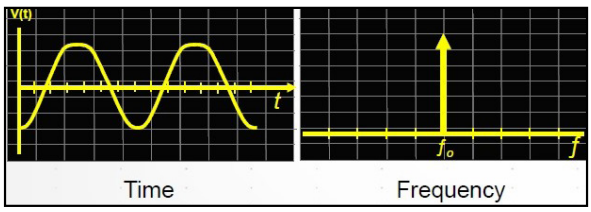

Figure 1a: Ideal Signal @ Time and Frequency Domain

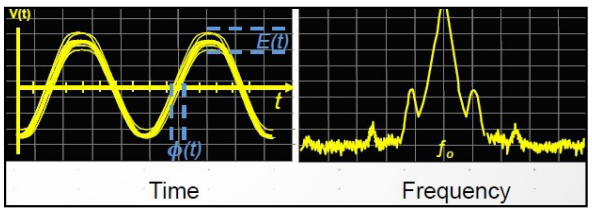

Figure 1b: Real Signal @ Time and Frequency Domain

Ideal Sinusoidal Signal
$V(t) = A_0 \sin(2\pi f_0 t)$
A_0 = Nominal Amplitude
f_0 = Nominal Frequency

Real Sinusoidal Signal
$V(t) = [A_0 + E(t)] \sin[2\pi f_0 t + \phi(t)]$
E(t) = Random Amplitude Fluctuations
ø(t) = Random Phase Fluctuations

The choice of domain is usually application dependent. Digital Design Engineers who work in Time Division Multiplexing (majority of modern telecom infrastructures) will be interested in jitter, as poor jitter performance will result in network slips and excessive re-send traffic. RF (Radio Frequency) Engineers working in Radar, Base Station designs etc. will be interested in Phase Noise as poor Phase Noise performance will affect up/down conversions and channel spacing.

JITTER

Jitter is the timing variations of a set of signal edges from their ideal positions in time. Rising and falling edges in a digital data stream never occur at an exact or desired timing location. Defining and measuring accurate timing of these edges will affect performance of synchronous communication systems. The edge displacement of a given signal, results in noise containing both spectral and power contents. These edges may vary randomly with respect to time as a result of non-uniform noise over the frequency domain (i.e. jitter caused by noise at a 10kHz offset could be greater or smaller than noise at a 100kHz offset). The spectral content of clock jitter may differ greatly based on the measurement technique used or bandwidth evaluated. Jitter in clock signals will contribute to the overall noise figure of a system. A high system noise figure will degrade performance and at times can disrupt its operation altogether.

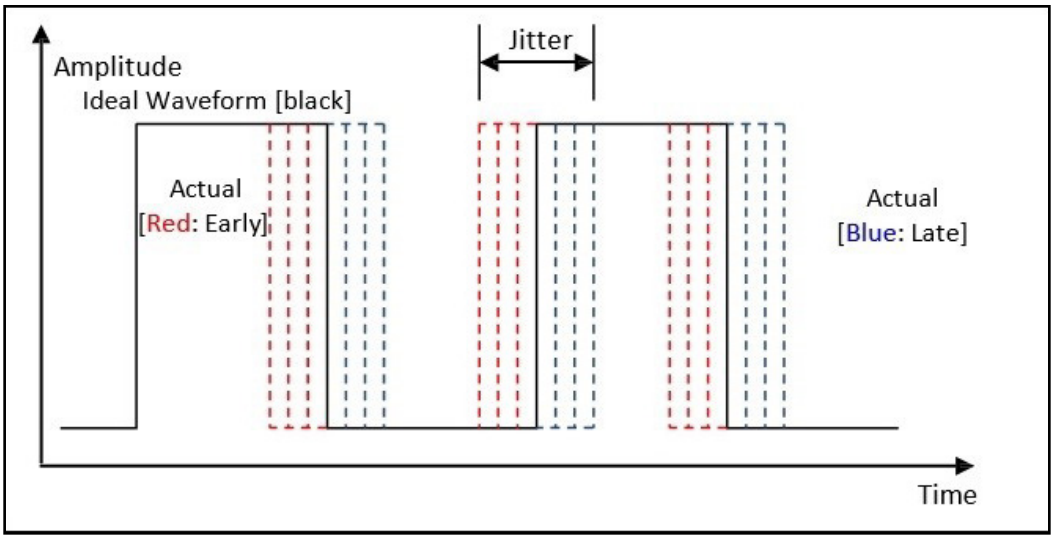

Figure 2: Jitter in the Signal

Jitter is categorized into two main types: **Deterministic Jitter [Dj]** and **Random Jitter [Rj]**. Dj can be divided into Periodic jitter (Pj) and Data Dependent jitter (DDj) which is composed of Duty Cycle Distortion (DCD) and Inter-Symbol Interference (ISI). The integration of all individual jitter components results in the total jitter (Tj), shown in Figure 3 on the next page. It includes contribution from all deterministic and random components.

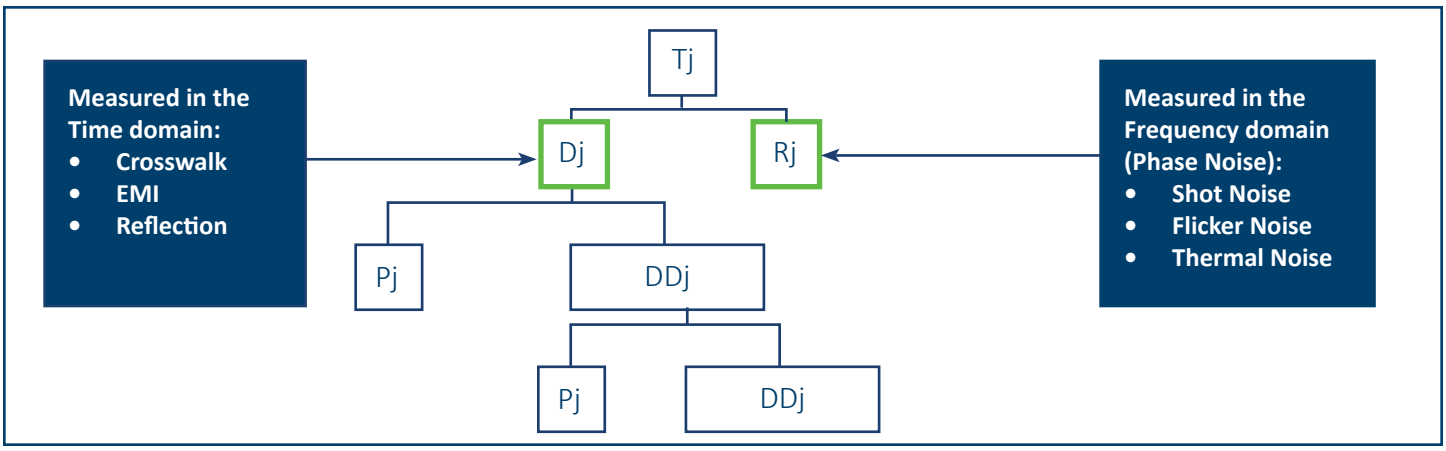

Figure 3: Total Jitter

Deterministic Jitter [Dj]

Dj is created by identifiable interference signals. Dj is predictable, consistent and has specific causes. It comes from system sources such as crosstalk, ISI (reflections) and power supply feed through Electromagnetic Interference (EMI). It has a non-Gaussian amplitude distribution that is always bounded which can be characterized by its peak-to-peak value. It is an artifact of board design and is typically controllable. Dj can be reduced by proper board design or IC selection.

Periodic Jitter [Pj]

Pj is cyclical resulting from a cross-coupling or EMI (AC power lines, RF signal sources, etc.) from a switching power supply. The latter is known as uncorrelated periodic jitter which couples into the data or system clock signal. A correlated periodic jitter is the coupling of an adjacent data signal from a clock of the same frequency. It is designated by a frequency and magnitude measured as a peak to peak number. Pj can be quantified using an oscilloscope.

Data Dependent Jitter [DDj]

DDj is divided into Duty Cycle Distortion (DCD) and Inter-Symbol Interference (ISI).

Duty Cycle Distortion [DCD]

DCD happens when the clock generates positive pulses that are not equal to negative pulses. It is the amount by which the mean positive width of cycles differs from the mean negative width. Amplitude offset errors, turn on delays, and saturation may be some of the causes of DCD.

Inter Symbol Interference [ISI]

ISI is sometimes referred to as data dependent jitter. It is usually the result of bandwidth limitation in the transmitter or physical media; therefore, creating varying amplitudes of data bits due to limited rise and fall times of the signal. It occurs when the frequency component of the data (symbol) is propagated at different rates by the transmission medium.

Random Jitter [Rj]

Rj describes timing variations caused by less predictable influences. It affects long-term device stability characterized by its standard deviation (RMS) value. It is generated from physical sources like thermal noise, white noise, and scattering in optical media. It can be characterized using Gaussian distribution statistics.

Common Sources of Deterministic Jitter

Electromagnetic Interface (EMI) results from conducted radiated emissions, undesirably radiated from local devices or systems. Common sources are switching type power supplies, which radiate strong, high frequency magnetic and electric fields, conducting a large amount of electrical noise into a system lacking adequate shielding and output filtering. EMI alters the biasing of electrical signals coupling or inducing noise currents in a conductor.

Crosstalk arises by accidental coupling of a magnetic and/or electric field to an adjacent conductor carrying a signal. The unwanted signal components are added to the original signal altering its bias determined by the amount of the interference signal.

Reflection is caused by the interfering of the original signal with components of itself, occurring when impedance mismatches exist in the channel. The optimal signal power transfer in copper technology happens when the medium has the same characteristic impedance at the transmitting and receiving ends of a system. If an impedance mismatch exists at the receiver, coming from uncontrolled stubbing and incorrect terminations, a portion of the energy is reflected back to the transmitter. However, if the mismatch is at the transmission end, the transmitter ingests part of the reflected energy while the receiver gets reflected the remainder. Ultimately, the receiver gets the delayed signal out of phase with the original one, being algebraically added with the first arriving signal.

Common Sources of Random Jitter

Shot Noise also known as broadband "white noise" is created by the movement of electrons and holes in a semiconductor whose amplitude is a function of the average current flow generated by fluctuations about its average value. In a semiconductor, it will depend in the randomness of the density of electrons and holes. It is a contributor of Rj in a signal channel.

Flicker Noise also known as pink noise is proportional to the reciprocal of the frequency, 1/f. It is only of concern in low frequency measurements. It is normally found in resistors, diodes, switches, and transistors among other components. Typically, it must be measured empirically.

Thermal Noise is the noise generated by thermal agitation of electrons moving freely within a conductor.

Measuring Jitter

There are three types of instruments being used to measure jitter.

1. BER (bit-error-rate)
2. Jitter Analyzers
3. Oscilloscopes

Time domain equipment, which effectively present period and cycle-to-cycle measurements, are used to measure jitter. Time domain equipment generally have a higher noise floor than frequency domain equipment

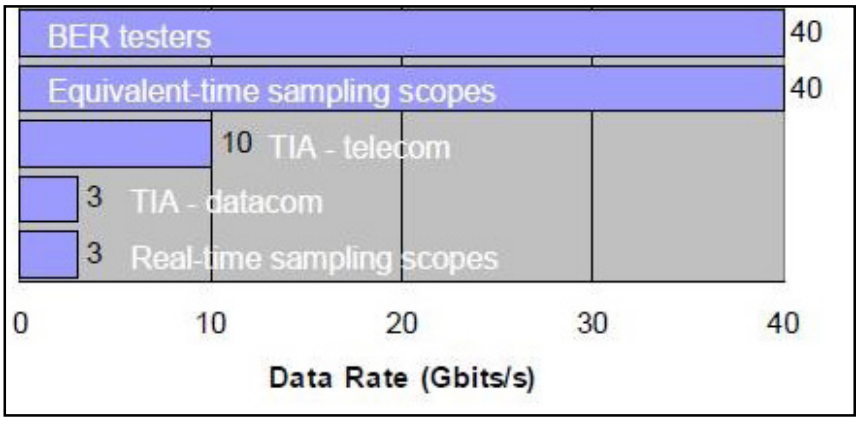

Figure 4: Measurement Data Rates

The type of instrument used to measure jitter will depend on the application; electrical/optical, datacom or telecom, and the bit rate (see Figure 4). A mix of these instruments may be needed to accurately track down a problem related to jitter.

The most common method is to start with a BER tester. To further isolate the problem, additional testing is done using a jitter analyzer or an oscilloscope. In addition to quantifying jitter, measurements should assist designers to investigate the root cause and source(s) of the problem to effectively eliminate jitter.

BER testers allow engineers to obtain an accurate measured bit error rate of a device under test. Devices used in high speed data communication buses like Fiber Channel, Serial ATA, InfiniBand and Rapid IO, benefit from using TIA testing. They are designed to sample every single bit received in a data stream comparing it against a predetermined pseudorandom bit sequence (PRBS) pattern. In most cases, jitter analyzers or oscilloscopes cannot achieve such accuracy.

Jitter Analyzers (Time Internal Analyzer) measure the interval from a reference clock to a signal edge or between threshold crossings, using histograms and collecting a large number of data points. TIA's are found in production line testing, because they can predict BER in a few seconds.

Oscilloscopes use an external trigger event and a sampling clock to build the eye diagram, by sampling over time a repetitive signal. The threshold crossing time of a signal is formed by a histogram allowing to measure jitter. An approximation of the jitter's probability density function (PDF) is derived from the histogram that can be examined to characterize jitter.

Real time sampling oscilloscopes are useful in testing subsystems, cables, devices or systems communicating at high speeds. These types of scopes measure jitter on any clock signal, not only the ones used in communications. To measure jitter at high bit rates in today's world, sampling oscilloscopes are the best choice due to their high bandwidth sampling capability. They require PRBS signals, which are repetitive due to their low sampling rate (150k samples/s or less), to generate eye diagrams in order to build a jitter picture.

Common Jitter Measurements

Cycle-to-Cycle Jitter [short-term jitter]

Cycle-to-cycle jitter is the maximum difference between two consecutive clock cycles. It is always specified as an absolute magnitude and not by positive or negative value. Cycle-to-cycle jitter is important for specifying the performance of a PLL; however it does not establish a relationship between non-adjacent clocks. Specifically, it does not address frequency drift over time.

Period Jitter [long-term jitter]

Period jitter is the difference between the position the clock cycle should be and the point at which it appears to be. It compares the length of each period to the average period of an ideal clock at a long-term average frequency of the signal. Period jitter is typically specified over a set number of clock cycles. JEDEC Specification, JESD65B, suggests measuring jitter over 10,000 cycles.

The standard deviation and the peak-to-peak (Pk-Pk) value are frequently referred to as the RMS value and the Pk-Pk period jitter. Because the period jitter from a clock is random in nature with Gaussian distribution, it can be completely expressed in terms of its Root Mean Square (RMS) value in pico-seconds (ps). However, the peak-to-peak value is more relevant in calculating setup and hold time budgets. The following equation is derived from the Gaussian Probability Density Function (PDF) table and can be used to convert the RMS jitter to Pk-Pk jitter for a sample size of 10,000.

Peak-to-Peak Period Jitter = 7.44 x (RMS jitter)

[Ex. RMS jitter is 2ps, the peak to peak jitter is ±14.88ps]

PHASE NOISE

The phase noise of an oscillator, at a given offset, is derived from the ratio of the power in a 1Hz bandwidth at the offset frequency to the total power of the carrier. Phase noise is generally considered the short-term phase/frequency instability of an oscillator or other RF/microwave components.

Single sideband phase noise $\mathcal{L}(f)$ is a relative power measurement.

$$\text{Phase Noise [dBc]} = \frac{\text{(Power Level of a 1Hz Band at Offset f)}}{\text{(Power Level of Carrier Frequency fc)}}$$

Figure 5 shows the frequency spectrum plot of a real sinusoidal clock with nominal frequency fc (also called the carrier frequency), plus sideband offset noise frequencies f. The complete power on the oscillator would be centered at f=fc, if the phase noise equals zero. However, phase noise spreads some of the power of the oscillator to adjacent frequencies resulting in sidebands.

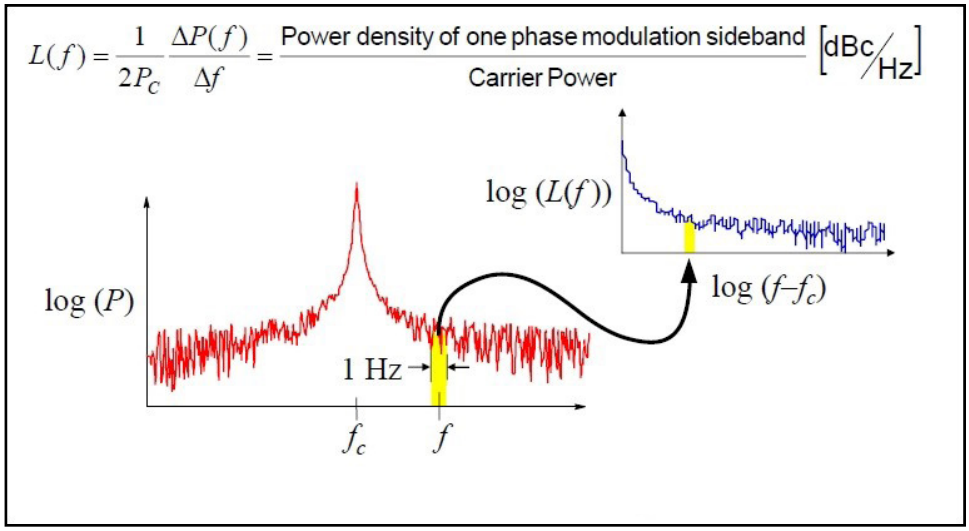

Figure 5: Frequency Spectrum

That means, sometimes the clock will have a slightly larger frequency fc + f and sometimes it will have a slightly lower frequency fc - f. The small changes in frequency appear as phase shifts in the clock waveform, hence the name phase noise. The actual units of Phase Noise are dBc/Hz because the power is normalized to a 1Hz bandwidth.

Measuring Phase Noise

Single Side Band (SSB) Phase Noise is also extracted from the frequency domain signal. In theory and with perfect measuring equipment, phase noise measured to an infinite carrier offset would provide the same value as jitter. However, using practical test equipment there will always be a discrepancy between the two. Furthermore, each measurement provides different views of the same phenomena, which are useful for seeing different types of jitter and frequency anomalies.

The power spectrum of the oscillator is represented in Figure 5 and a noisy phase angle term, called the spectral density of the phase fluctuations, is represented in Figure 6. The measurement of the spectral density of phase variations, in Figure 6, is the same as the phase noise in dBc/Hz measured from the power spectrum, in Figure 5, for offsets very far from the carrier.

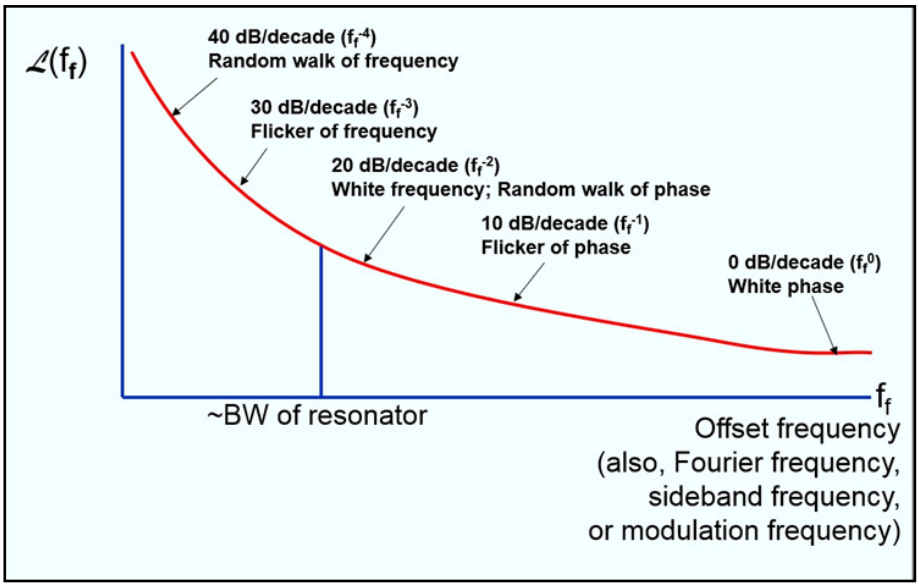

Figure 6: Phase Noise. Source: John R. Vig Tutorial

Phase Jitter [Integrated Phase Noise]

Phase jitter is measured by integrating the phase noise across specified frequency offsets from the carrier signal. Phase jitter measures the amount of energy present in the specified frequency offsets from the carrier signal compared to the energy of the carrier signal by integrating the area under the phase noise plot. SONET uses a frequency offset of 12kHz to 20MHz from the carrier signal to integrate the area under the phase noise plot, to measure phase jitter. See Figure 7.

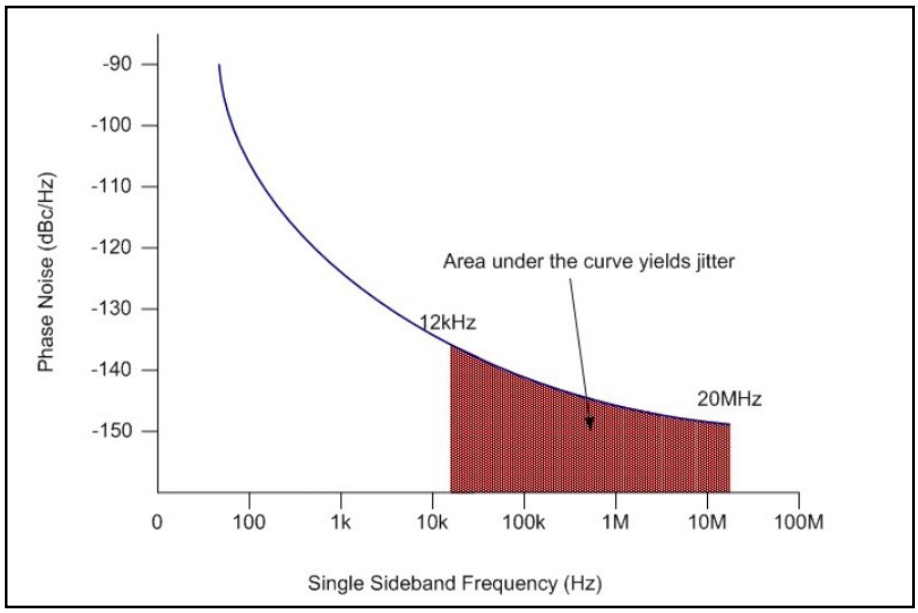

Figure 7: Phase Jitter

The power spectral density function in dBc is the sideband noise propagation given by the plot. As the associated levels of phase noise (modulation) are reflected by jitter, the power level of the carrier is of no importance. The result of the integration (f) across the specified bandwidth, 12kHz to 20MHz, is the overall noise power of the sidebands. The RMS jitter can be derived by calculating the power level of the phase modulation in this band. When jitter is derived from phase noise plots, the sideband frequency interval over which it is calculated must always be specified.

RMS Jitter Calculation Example:

RMS jitter value of a 312.5MHz oscillator can be calculated as below:

$$N = \text{Noise Power [dBc]} = \int_{12kHz}^{20MHz} \mathcal{L}(f)df = -63dBc$$

From the noise power N, RMS Phase Jitter value in radians can be calculated using this formula:

$$\text{RMS Phase Jitter [radians]} = 2x\sqrt{10^{N/10}} = 2x\sqrt{10^{-63/10}} = 0.001416 \text{ radians}$$

The jitter value in radians can be converted to RMS jitter in time units of seconds:

$$\text{RMS Jitter [secs]} = \frac{\text{Jitter [Radians]}}{2\pi f} = \frac{0.001416}{2\pi 312.5Mhz} = 0.72 \text{ Pico seconds [RMS]}$$

Figure 8 shows an example of phase noise and phase jitter measurement of a CTS Model 637 crystal oscillator, which generates an LVPECL output at 156.25MHz, meeting the jitter requirements of SONET applications.

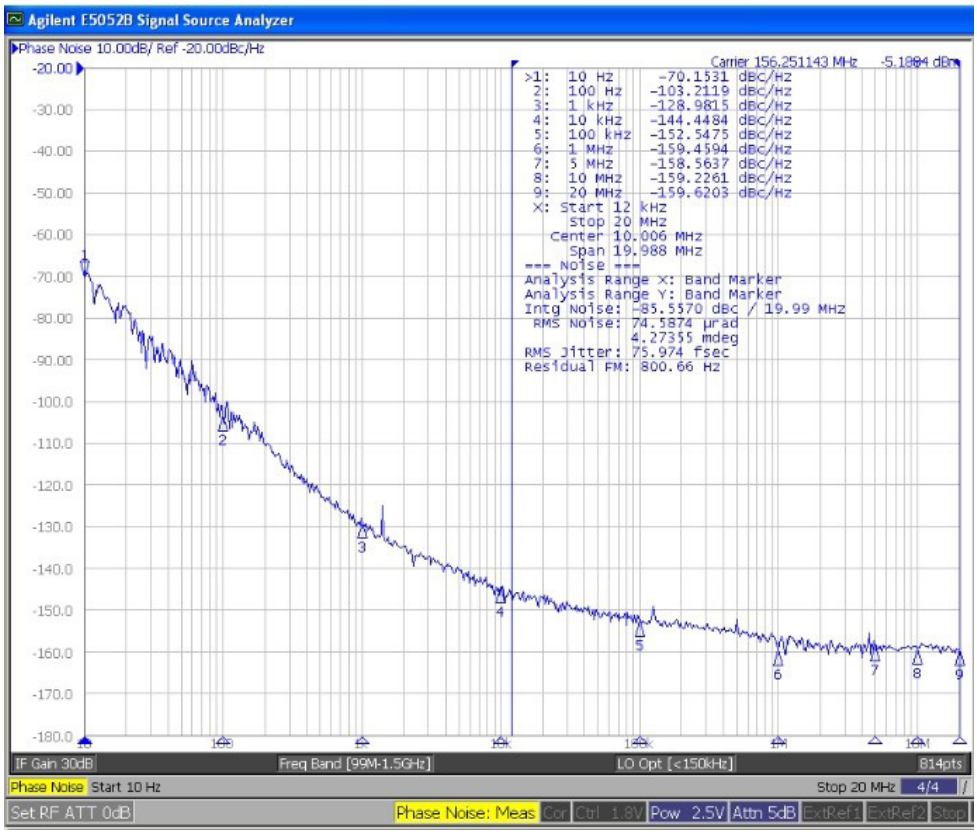

Figure 8: CTS 156.25MHz LVPECL Output Oscillator

Minimizing Phase Noise

It is typical for customer applications to become more demanding as data rates increase. With the increasing system data rates, timing jitter has become critical in system design, as in some instances the system performance limit is determined by the system timing margin. The phase noise of oscillators can lead to erroneous detection of phase transitions, i.e., to bit errors, when phase shift keyed [PSK] digital modulation is used.

The main part of phase noise in a crystal oscillator is determined by the Q value and signal level of the crystal and the noise performance of the oscillation circuit. When improving the phase noise performance near the carrier frequency of phase noise, the Q value of the crystal plays a particularly important role. The higher the signal level is, the lower the phase noise level becomes regardless of the offset frequency. Phase noise can be lowered by setting the signal level at as high a value as the system allows. However, the upper level of excitation applicable to a crystal is limited. An excessively high excitation level may cause unnecessary oscillation modes to occur, with the oscillation becoming abnormal.

Shock and vibration can produce large phase deviations even in "low noise" oscillators. Low noise, acceleration insensitive oscillators are essential in such applications. In recent years, due to increasing amount of data transmitted, crystal oscillators used in electronic information and communication equipment, are required to further improve the noise performance and increase the clocking speed of the reference signal.

For well-designed quartz crystal oscillators with output frequencies at the frequency of oscillation of the crystal, the jitter should arise solely from random noise source.

There are two key techniques that can be implemented by designers to reduce deterministic signal jitter.

Fully Differential Signaling
Differential signaling conventions such as LVDS, PECL or HCSL greatly reduce the effects of deterministic jitter. Any interference or crosstalk experienced on a signal path will also be picked up by its differential path. The high common noise rejection of such signaling systems tends to cancel out jitter.

Conductor Trace Routing
In an application design, conductor traces should be as short as possible, and should not cross paths that are carrying fast switching digital signals. The higher frequencies deployed in systems cause long PCB traces to behave like transmission lines, due to the associated fast edge rates. Maintaining a balanced system requires proper termination techniques for the trace routings in the application. Wherever possible, avoid stray signals that may be imprinted on to the signal track as a result of crosstalk or interference. If a differential signaling system is used, the two paths should stay as close as possible to each other so as to take advantage of their inherent common mode noise rejection.

CTS SOLUTIONS

CTS has solutions that provide low jitter differential clocks portfolio, providing design engineers with high performance solutions, low cost options, and miniature package sizes suitable for complex electronic systems. These series of clock models support a wide array of market segments; covering infrastructure telecommunication networking, server applications, test and measurement, medical test equipment and much more; delivering superior low phase jitter performance, a high level of frequency stability, with an extended temperature range option covering -40°C to +105°C, targeting applications operating in fan-less enclosures and industrial environments.

CTS offers cost effective, small package solutions, along with high performance capabilities, suitable for complex electronic system requirements. Several Stratum 3 TCXO models (i.e. Models 580 and 581) support a wide array of applications, covering 1588 timing and synchronous Ethernet, base stations including femtocells and microcells, networking, test and measurement, and many more. They deliver outstanding phase noise performance and a high level of frequency stability.

CTS enables 5G infrastructure through its high-performance product lines of ultra-low noise precision timing devices and RF ceramic filters that support both sub-6 GHz and mmWave wireless infrastructure. CTS' 5G product portfolio is designed to comply and support stringent performance and quality standards of networking systems' wider bandwidth and transmission rates operating at high frequencies, powering applications such as 5G mass MIMO base stations, small cells, and mmWave 5G hybrid beam forming base stations.

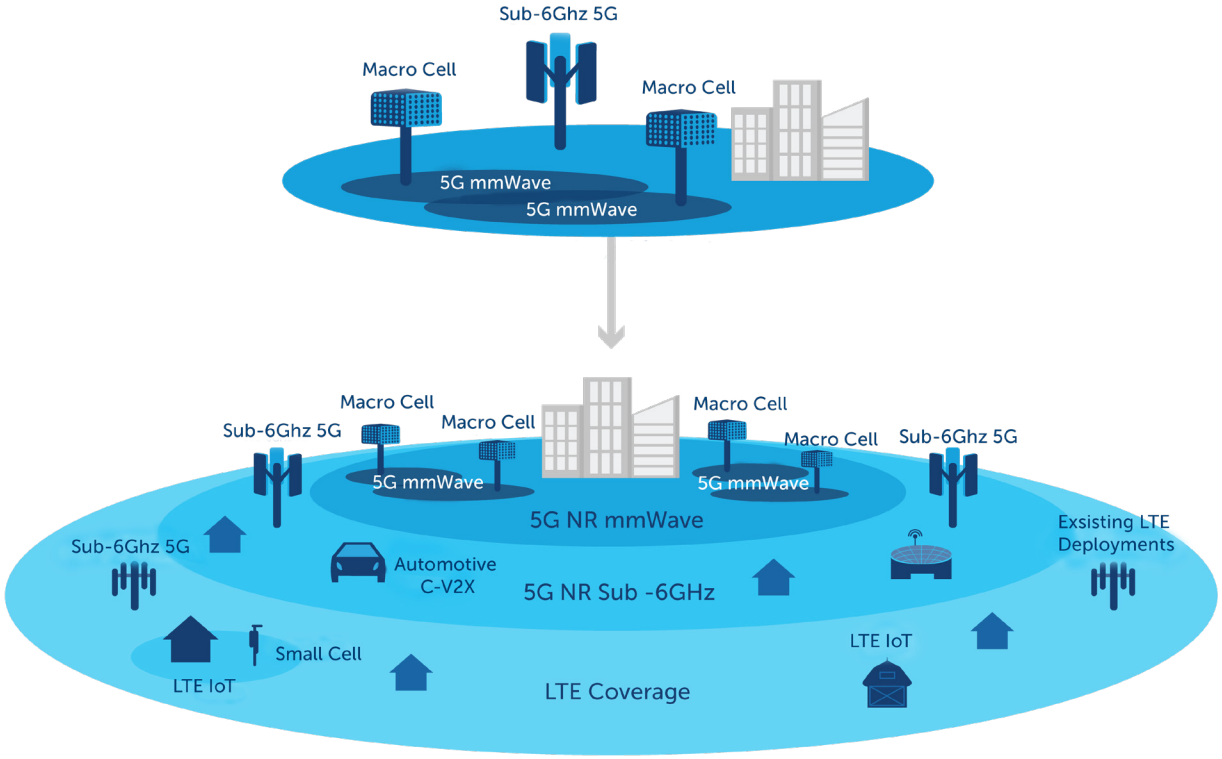

Figure 9: 5G Infrastructure

CTS precision timing devices for 5G networks utilize low noise frequency synthesis techniques to clean system noise and multiply low frequency to high frequency making our technology suitable for high transmission rates. Our embedded ASIC solution and high Q crystal technology offer optimized signal to noise ratio that results in a precise and clean signal that is used for data, voice, and video transmission. Reference the CTS 5G Market website page, linked in the More Information and Other Content section of this paper.

CTS provides excellent frequency stability crystals and crystal oscillators, which are used as high-quality signal sources for clocks in many types of electronic equipment. Crystals or crystal oscillators excel not only in long-term or static stability such as frequency stability, temperature characteristics, and aging characteristics, but also in short-term high stability represented by the phase noise and jitter performance thanks to high Q-values of crystals.

CONCLUSION

In the development and integration of communication systems, high-speed digital designers need to consider the jitter and phase noise contribution of the frequency reference, when evaluating the timing budget for the overall system. As technology advances, speeds increase, and connectivity widens; clock oscillators and other timing components that support these applications must provide best in class timing references with low noise. CTS supplies high quality products along with the smartest solutions at a quality price. Please contact CTS to discuss your timing needs to get the best and most economical solution for your application.

ENGINEERING CONSULTATION

CTS provides complimentary consultations with one of our specialized design engineers to assist you in designing your embedded technology-based product or system.

Picking the right frequency control component is critical for success. Comparing hundreds of available frequency control components is time consuming. Consult a CTS engineer to save time in evaluating the right component for your project.

Leverage our engineering expertise. We encourage you to tap into our engineers' collective knowledge base to solve your most complex design issues and find the best solution to meet your needs, no matter the application.

With a comprehensive portfolio of frequency control components, our engineers have a vast foundation of solutions to meet your requirements. However, if you need turnkey product development or a custom configuration to fit a specific application, our engineers are available to consult with you on how CTS can fulfill custom modifications to your meet your project specifications.

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