

Model 615

HCMOS Clock Oscillator

Features

- Plastic Surface Mount Package
- Good Phase Jitter Performance, 700fs Typical
- Fundamental and 3rd Overtone Crystal Designs
- Frequency 1 - 160MHz
- +3.3V and +5.0V Operation
- Operating Temperature -40°C to +85°C
- Output Enable Standard
- Tape and Reel Packaging, EIA-481



Part Dimensions:
14.0 × 9.0 × 4.7mm • 1,182.02mg

Description

Plastic 9x14mm, J-lead, clock oscillator designed specifically as a form-fit-function replacement for the old, obsolete ceramic packaged class of J-lead clock oscillators.

Ordering Information

Model	Supply Voltage	Frequency Stability	Temperature Range	Frequency Code [MHz]	Packaging																
615	L	3	C	XXXMXXXXX	T																
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Notes:

- 1] Consult factory for availability of 6I Stability/Temperature combination.
- 2] Frequency is recorded with 3 leading digits before and 5 significant digits after the "M" [including zeroes].
[Ex. 3.579545MHz = 003M57954; 14.31818MHz = 014M31818; 25MHz = 025M00000; 125MHz = 125M00000]

This product is specified for use only in standard commercial applications. Supplier disclaims all express and implied warranties and liability in connection with any use of this product in any non-commercial applications or in any application that may expose the product to conditions that are outside of the tolerances provided in its specification.



Electrical Specifications

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.5	-	7.0	V
			2.97	3.30	3.63	V
			4.50	5.00	5.50	
Typical @ Nominal V_{CC} , $C_L = 15$ pF, $T_A = +25^\circ\text{C}$						
Supply Current	I_{CC}	@ +3.3V	-	-	35	mA
		@ +5.0V	-	-	45	
Output Load	C_L	-	-	-	15	pF
Operating Temperature	T_A	-	-20	+25	+70	
			-40		+85	
Storage Temperature	T_{STG}	-	-55	-	+125	$^\circ\text{C}$

Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range	f_0	-		1.0 - 160.0		MHz
Frequency Stability [Note 1]	$\Delta f/f_0$	-		20, 25, 50, or 100		$\pm\text{ppm}$
Aging	$\Delta f/f_{25}$	First Year @ +25 $^\circ\text{C}$, nominal V_{CC}	-5	± 3	5	ppm

1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		HCMOS		-
Output Voltage Levels	V_{OH}	Logic '1' Level, CMOS Load	0.9 V_{CC}	-	-	V
	V_{OL}	Logic '0' Level, CMOS Load	-	-	0.1 V_{CC}	
Output Current Levels	I_{OH}	$V_{OH} = 90\%V_{CC}$ [+3.3V, +5.0V]	-	-	-16	mA
	I_{OL}	$V_{OL} = 10\%V_{CC}$ [+3.3V, +5.0V]	-	-	16	
Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
Rise and Fall Time	T_R, T_F	@ 10%/90% Levels, Nominal V_{CC} , $C_L = 15$ pF				
		@ +3.3V	-	-	6	ns
		@ +5.0V	-	-	8	
Start Up Time	T_S	Application of V_{CC}	-	2	5	ms

Output Enable

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Enable Function		Standby				
Enable Input Voltage	V_{IH}	Pin 1 Logic '1', Output Enabled	0.7 V_{CC}	-	-	V
Disable Input Voltage	V_{IL}	Pin 1 Logic '0', Output Standby	-	-	0.3 V_{CC}	V
Standby Current	I_{STB}	Pin 1 Logic '0', Output Standby	-	-	10	μA
Enable Time	T_{PLZ}	Pin 1 Logic '1'	-	-	5	ms
Phase Jitter, RMS [Note 2]	t_{jrms}	Bandwidth 12kHz - 20MHz	-	0.7	1.0	ps
	p_{jrms}	-	-	-	5.0	
	p_{jpk-pk}	-	-	-	25.0	

2.] For frequencies 40MHz or less, the measurement Bandwidth is 12kHz - 5MHz.

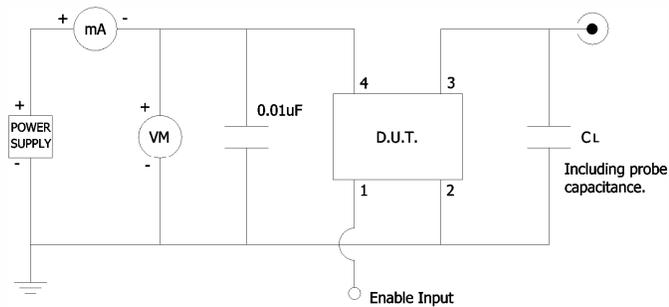
Electrical Specifications

Enable Truth Table

Pin 1	Pin 3
Logic '1'	Output Enabled
Open	Output Enabled
Logic '0'	Output Disabled, High Impedance

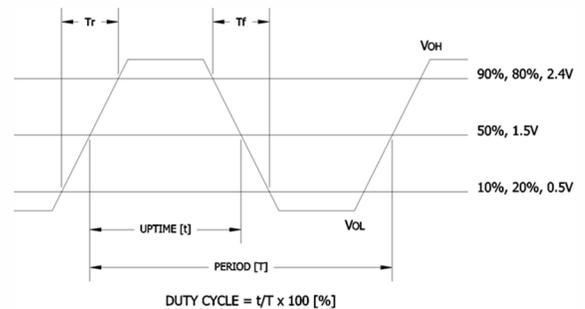
Test Circuit

CMOS



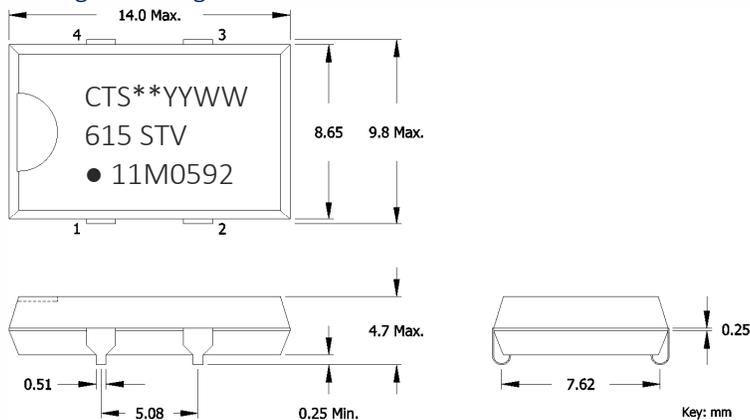
Output Waveform

CMOS

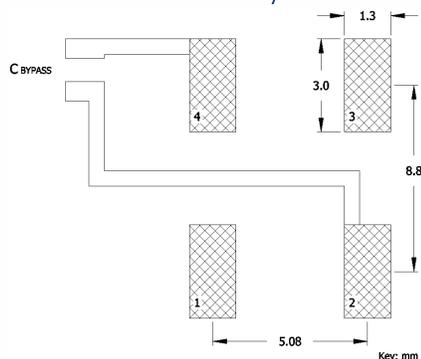


Mechanical Specifications

Package Drawing



Recommended Pad Layout



Marking Information

- ** – Manufacturing Site Code.
- YYWW – Date Code, YY = year and WW = week.
- STV - Frequency Stability/Temperature Code.
[Refer to ordering information for code]
V - Voltage Code: 3 = +3.3V, 5 = +5.0V.
- - Pin 1 Identifier.
- 11M0592 – Frequency is marked with only Leading significant digits before the 'M' and 4 digits minimum after the 'M' [including zeros].

Pin Assignments

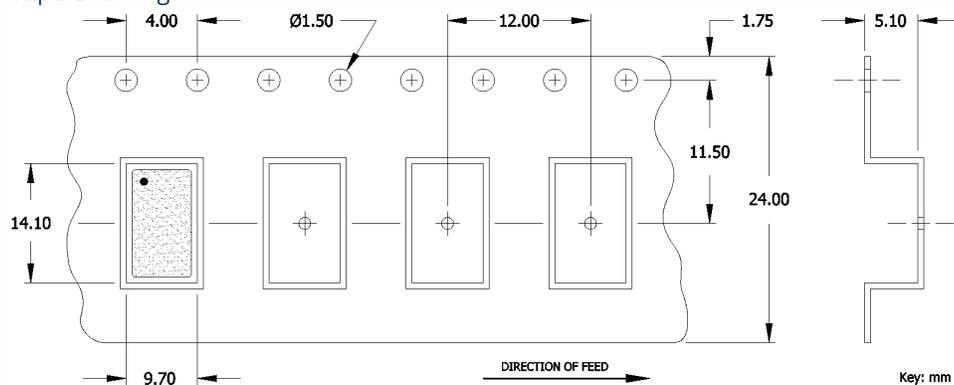
Pin	Symbol	Function
1	EOH	Enable
2	GND	Circuit & Package Ground
3	Output	RF Output
4	V _{CC}	Supply Voltage

Notes

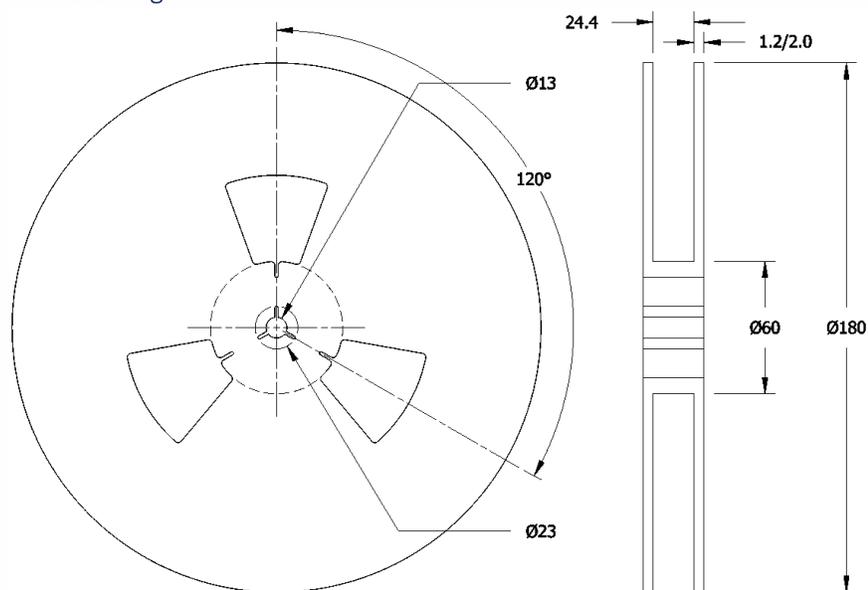
- JEDEC termination code (e4). Base metal is copper [Cu] with silver [Ag] plating.
- Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
- MSL = 1.

Packaging - Tape and Reel

Tape Drawing



Reel Drawing



Notes

1. Device quantity is 1k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value, date code and manufacturing site code information must appear on reel and carton labels.