DDR Memory Signal Termination

Introduction

The goal when terminating Double Data Rate (DDR) memory signals is to maintain signal integrity. The board designer must properly terminate the signal lines and make efficient use of layout space to meet this goal. By choosing BGA termination arrays with the proper impedance values, the designer can accomplish this goal.

Termination Standards for DDR Memory

The termination style required is based on the DDR memory application. Two classes of termination that meet the requirements of EIA/JEDEC Standard JESD8-9A for proper signal handling are shown in Figures 1 and 2. The 2.5V I/O memory bus standard operating in the logic switching range of 0.0 to 2.5 volts is SSTL_ 2. This standard is for high-speed DDR SDRAM interfaces.

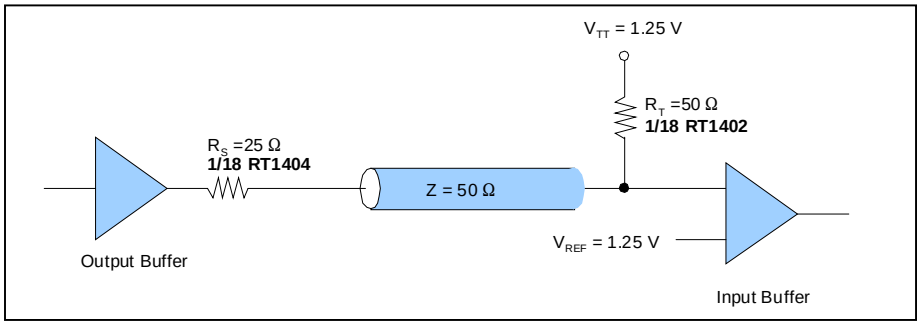

Figure 1. SSTL_2 Class I Termination

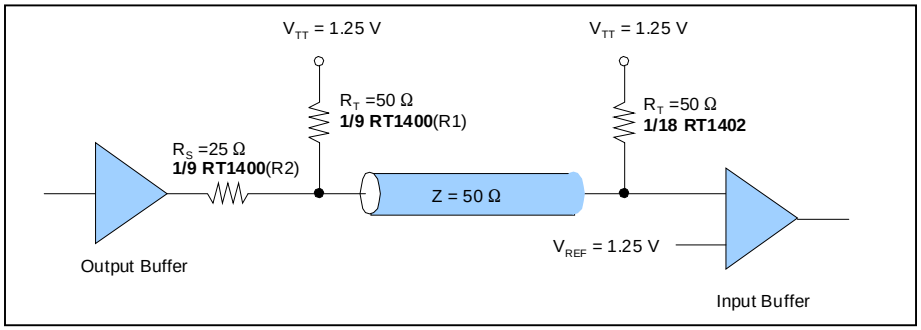

Figure 2. SSTL_2 Class II Termination

Either termination method can take advantage of compact routing made available with the BGA style package. It is recommended that the Class I resistor termination method be used for best performance. It reduces component count/placements and board space required, while providing simpler signal routing, reduced reflections, and better bandwidth and settling.

V_{TT} equals V_{REF} and is equal to 50% of V_{DD}. V_{TT} must maintain less than .040 volts offset from V_{REF} at all times. Decoupling with multiple parallel capacitors is recommended and special attention to minimize ESR and ESL should be considered.

Guidelines for Termination Layouts

Termination resistors should be placed as close as possible to the dual in-line memory module (DIMM) socket to minimize signal routing length. If using resistor arrays or a BGA network with only termination resistors, the bi-pass capacitors should be placed between the V_{TT} Termination Island and the V_{SS} plane with a minimum of one .01µF capacitor, spaced evenly, for every two termination resistors. With either method of termination, the PCB should include a 10µF tantalum capacitor at each end of the termination island for bulk decoupling.

An example of a complete termination solution utilizing a BGA package with termination resistors and bi-pass capacitors is shown in Figure 3.

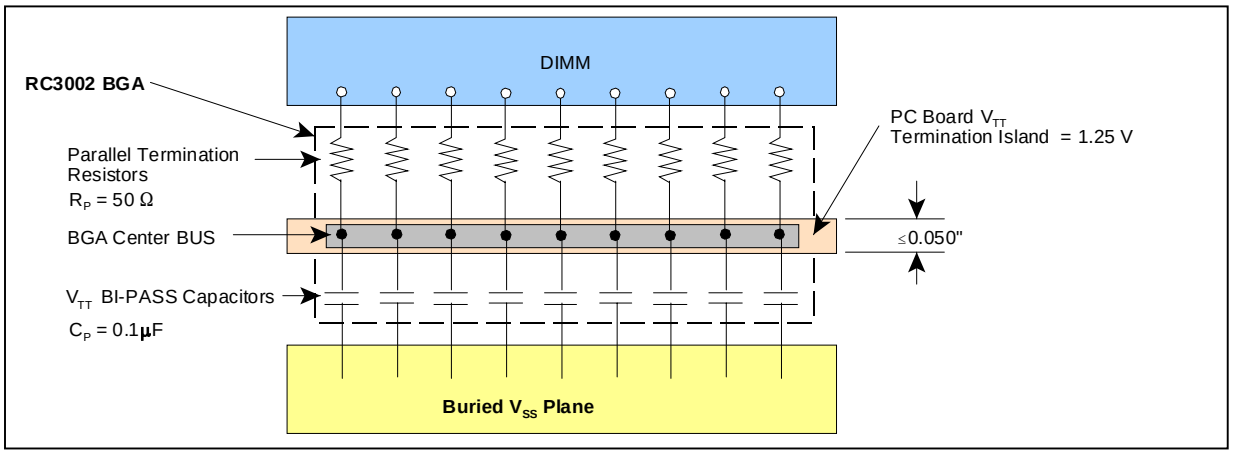

Figure 3. DDR Signal Termination Example with RC3002 BGA

Figure 3 demonstrates the advantage of having bi-pass capacitors integrated into the BGA part. The designer should incorporate a 0.050" wide V_{TT} Termination Island on the top PCB layer to optimize the printed circuit board (PCB) layout and routing. The V_{SS} plane is on a lower buried PCB layer and should have no slots, if possible.

Guidelines for PCB Routing

The recommended BGA routing schemes for the 1.27mm and the 1.00mm pitch terminators are shown in Figure 4.

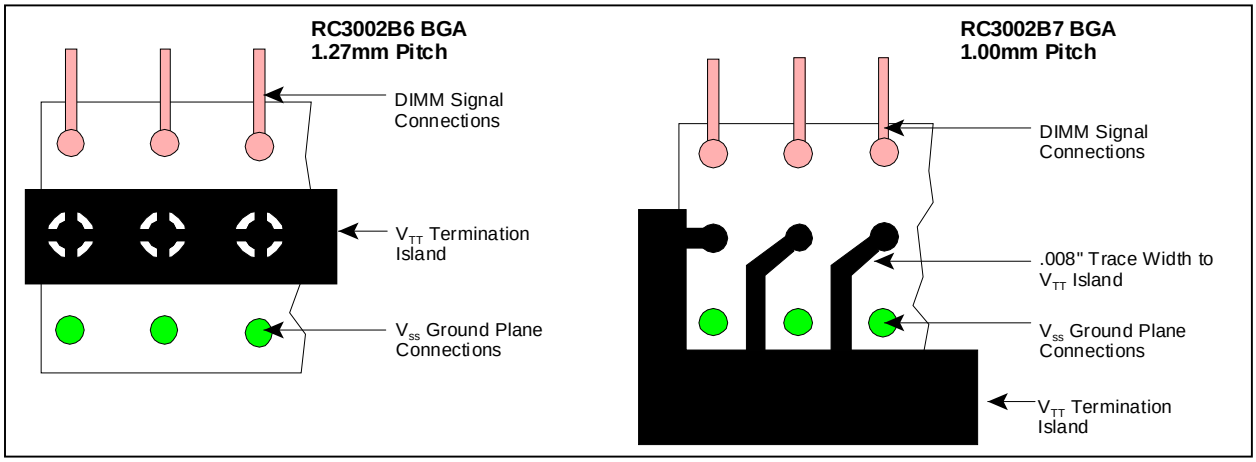

Figure 4. Routing Schemes for 1.27mm and 1.00mm RC BGA Terminations

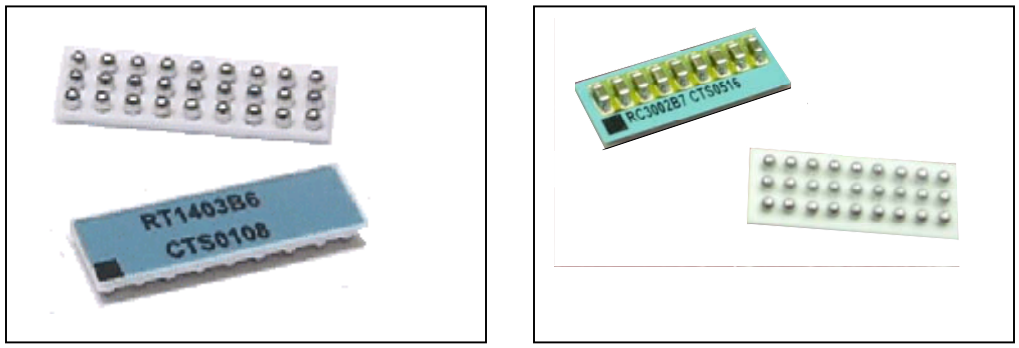

Figure 5. RT1403B6 Resistor Terminator and RC3002B7 Resistor/Capacitor Terminator

Conclusion

DDR memory termination solutions can be solved very efficiently with proper component selection and careful attention to placement and routing techniques. The BGA resistor or resistor/capacitor terminators provide the most efficient means for accomplishing this task.

Referenced Documents

SSTL-2 Class I & II – EIA/JEDEC Standards JESD8-9A

Application Notes:

Printed Circuit Assembly Guidelines	AN-C1-PCAG-A
ClearONE Rework Procedure	AN-C1-RW-A
ClearONE RC BGA Rework Procedure	AN-RC1-RW-A

Link to DDR SDRAM Terminator Data Sheet:

http://www.ctscorp.com/components/clearone.asp

Link to Application Notes:

http://www.ctscorp.com/components/clearone/appnotes.htm

Link to RC BGA Data Sheet:

http://www.ctscorp.com/components/clearone.asp

Written by: Damon Niswonger
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