

CTS Front End Module Application Note

INTRODUCTION

The VFM1004A is a RF front end module for a 3G picocell. The module utilizes distributed filtering with three filters: duplexer, receive bandpass filter and transmit bandpass filter. The VFM1004A also includes a power amplifier, a low-noise amplifier and other necessary RF components. In the transmit path, it can deliver 24 dBm WCDMA power at the antenna port, while achieving a typical ACLR (Adjacent Channel power Leakage Ratio) of -50 dBc with a PAR (peak to average ratio) of 8 dB.

The VFM1004A targets the 3G Wideband CDMA market, specifically UMTS. Superior filtering, Tx/Rx isolation, and power management are achieved in the design of these modules.

The VFM1004A, which has a patent pending, is designed to meet the 3GPP Release 6 specifications. It can replace all of the RF components that would be typically used in a UMTS Node B local area front end. It is compliant to TS25.104 R6. The design is also flexible to enable customers to select different values for receiver sensitivity, selectivity and output power. It is RoHS compliant and lead-free. The front end module is shown in Fig. 1.



Fig. 1

Some features of the front end module include:

- Scalable power amplifier capable of delivering 24 dBm at the antenna port
- Distributed filters offering excellent isolation and harmonic suppression
- A low noise amplifier with a bypass mode to increase receiver linearity

The front end module block diagram is shown in Fig. 2. The receive section is the top path. The transmit section is the bottom path. The receive section is under the metal lid and the transmit section is mainly exposed to minimize heat build up under the lid.

Simplified block diagram

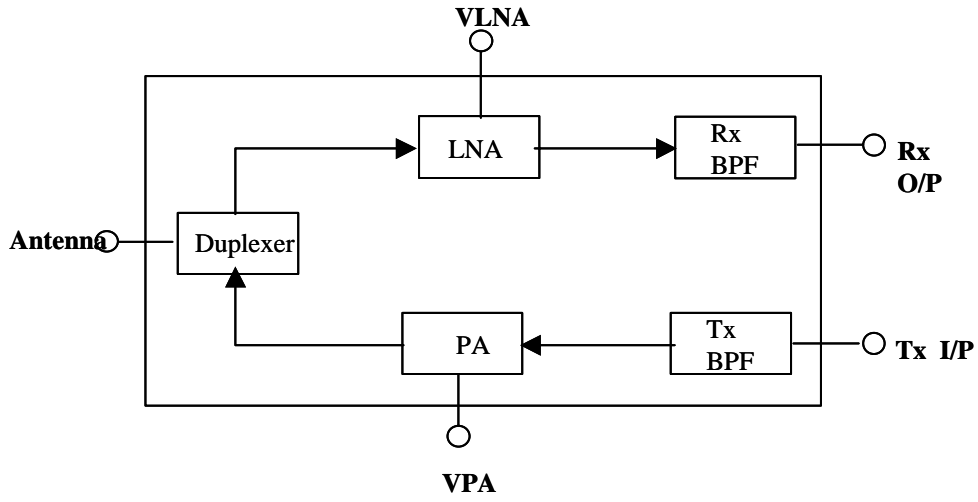
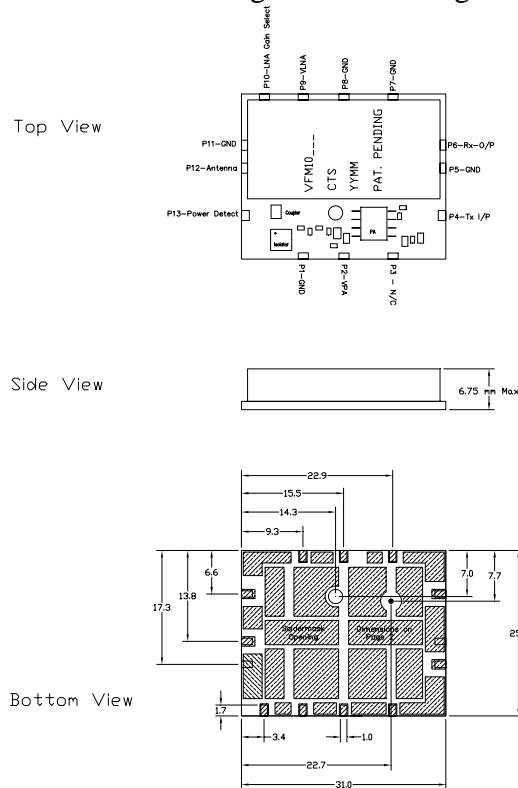


Fig. 2

MECHANICAL CONSIDERATIONS

The front end module mechanical drawing is shown in Fig. 3.



All Dimensions are in Millimeters

Fig. 3

The following graph shows Tx and Rx Gain @ the antenna.

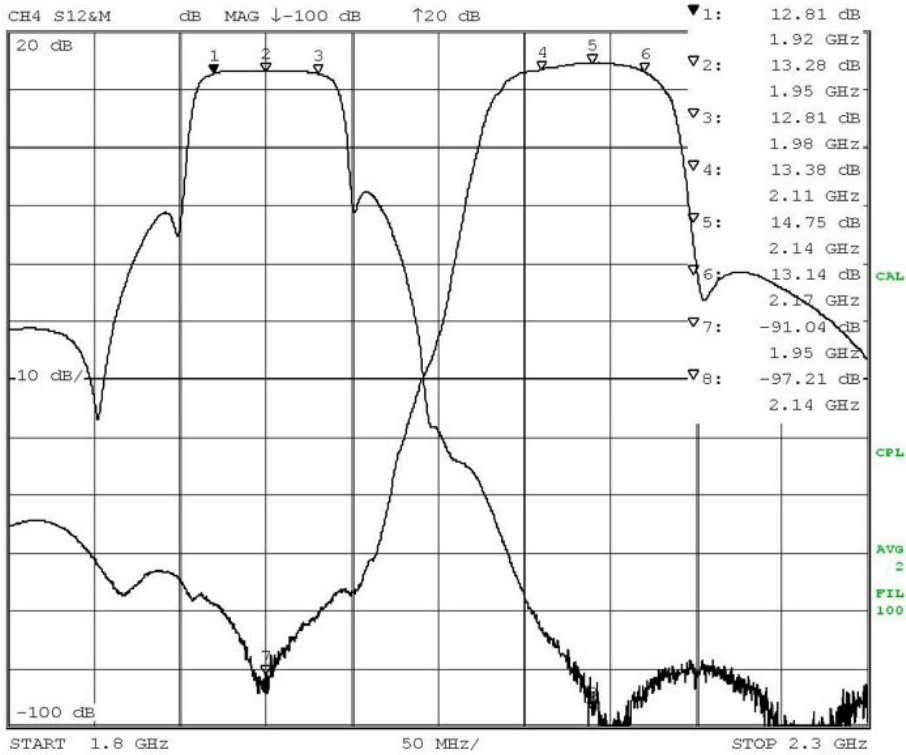


Fig. 4

The following graph shows the ACLR.

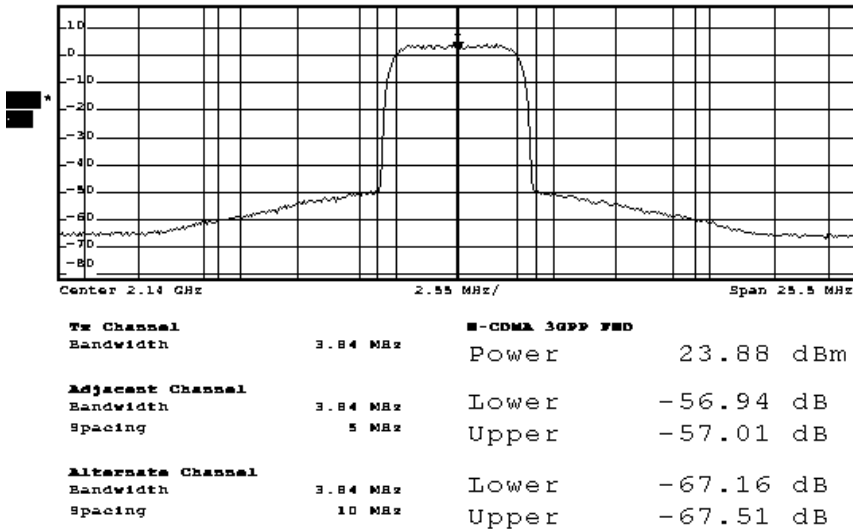


Fig. 5

THERMAL CONSIDERATIONS

Thermal management of the front end module is an important element in system reliability. The front end module PCB has many metallized vias under the power amplifier. The PA has a junction-to-case thermal resistance (Θ_{jc}) of approximately 9.5°C/watt. At full power, the PA dissipates 7.25 watts of heat. The maximum ΔT of the PA junction to case would be (7.25 watts)(9.5°C/watt) = 68.9°C.

It is recommended that a hole is created in the customer's motherboard so that the heatsink is in direct contact with the module PCB. There is a hole in the front end module next to the PA. This hole is to accommodate a screw to affix the module to the motherboard and to the heatsink. The hole diameter is 2.06 mm (.081"). With the module and customer PCB fastened to the heatsink with a screw, the effective thermal resistance will drop considerably.

For heatsink requirements, we recommend that you contact:

Intl. Electronic Research Corp. (IERC)
413 N. Moss St.
Burbank, CA 91502
(818) 842-7277
www.ierc.net

TESTBOARD

The front end module testboard is shown in Fig. 6.

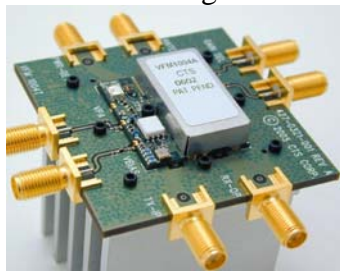


Fig. 6

The FEM testboard kit, VFM1004T, also comes with SMA cables for DC connections.