ClearONE Termination Solutions for Interfacing 2.5 Volt LVPECL Drivers and Receivers

INTRODUCTION

Interfacing low voltage communication data signals requires linking devices without causing signal degradation. Both transmitting and receiving devices must be terminated properly to insure that the data being transmitted is not corrupted at the receiver. The Xilinx Vertex-II Pro/X family of Field Programmable Gate Arrays (FPGA) when used with an LVPECL (Low Voltage Positive Emitter Coupled Logic) differential I/O, requires unique termination to insure signal integrity.

LVPECL Termination Requirements

An LVPECL transmitter termination consists of a series-shunt combination for each differential pair. A typical externally terminated LVPECL transmitter is shown in Figure 1. The resistor values are selected to maintain a standard ±350mV signal swing.

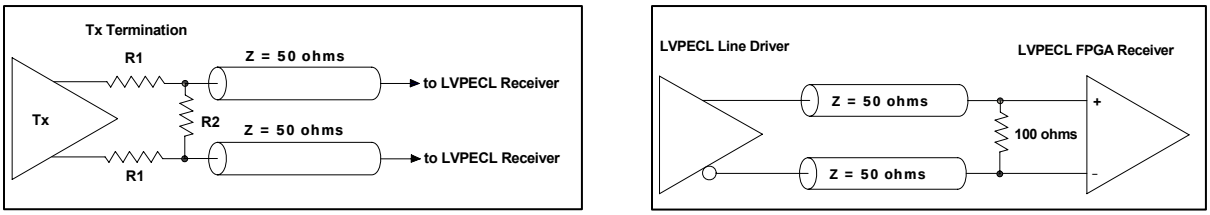


Figure 1. LVPECL External Transmitter & Receiver Termination Examples

Applications

Each LVPECL data bus signal pair requires either internal or external termination. For FPGA product families that require external termination, ClearONE BGA terminators provide a simple solution for board layouts. ClearONE BGA terminators provide the performance necessary to insure the signal integrity is maintained by the data bus. The Xilinx Virtex-II Pro or Virtex-II Pro X FPGA are examples of devices requiring external termination.

The Virtex-II Pro or Virtex-II Pro X LVPECL transmitter driving 50Ω transmission lines into a 2.5V LVPECL receiver requires the typical resistor values shown in Figure 2. The figure illustrates the recommended termination technique for interfacing Xilinx differential receivers, following the 2.5V differential standards, by placing a 100Ω termination between the receiver inputs.

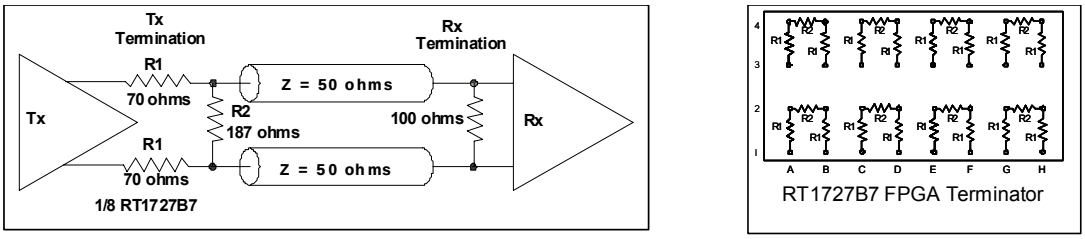


Figure 2. 2.5V LVPECL External Termination Receiver & Transmitter Circuit

An often preferred technique for terminating LVPECL transmission lines is the Thevenin Equivalent circuit solution. The typical application requires that the data bus lines be terminated to V_{CC} and V_{EE} through resistors, as shown in Figure 3.

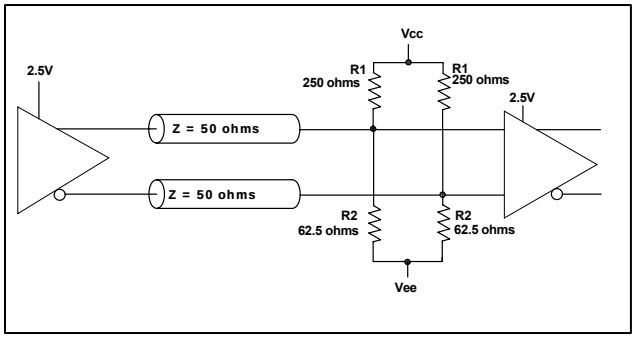


Figure 3. 2.5V LVPECL Parallel Termination-Thevenin Equivalent

Tables 1 & 2 list CTS ClearONE part numbers that can be used for the transmitter/receiver 2.5V LVPECL resistor terminations with the Xilinx Vertex-II Pro/X series FPGA's. Custom versions of ClearONE terminators can be developed for FPGA's requiring unique transmitter or receiver terminations to maintain signal integrity.

Part Number	R1 Ω	R2 Ω	Array Size	Pitch (mm)	RoHS Part Number
RT1710B6	100	N/A	4 x 8	1.27	RT2710B6
RT1710B7	100	N/A	4 x 8	1.00	RT2710B7
RT1726B7	70	187	4 x 16	1.00	RT2726B7
RT1727B6	70	187	4 x 8	1.27	RT2727B6
RT1727B7	70	187	4 x 8	1.00	RT2727B7
RT1728B7	70	240	4 x 16	1.00	RT2728B7
RT1729B6	70	240	4 x 8	1.27	RT2729B6
RT1729B7	70	240	4 x 8	1.00	RT2729B7

Table 1. ClearONE standard Part Numbers available for LVPECL Termination

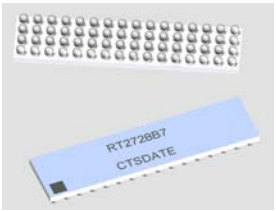
Part Number	R1 Ω	R2 Ω	I/O	Pitch (mm)	RoHS Part Number
RT1251B6	250	62.5	8	1.27	RT2251B6
RT1251B7	250	62.5	8	1.00	RT2251B7

Table 2. ClearONE Thevenin Terminators for 2.5V LVPECL

SUMMARY

The CTS ClearONE family of BGA terminators offer efficient solutions for board layout on LVPECL transmitter/receiver circuitry using the Xilinx Vertex-II Pro/X series FPGA's. ClearONE terminators offer the lowest parasitic I/O capacitance and inductance solutions available. Custom resistor values and tolerances are available upon request.

Additional CTS ClearONE product information can be found at:
http://www.ctscorp.com/components/



Written by: Damon Niswonger
Date: October 9, 2007