VFCG-HD1
Synchronous Clock Generator
For HD and SD Video Broadcast

Valpey Fisher Corporation
High Frequency, Low Phase Noise Timing Solutions

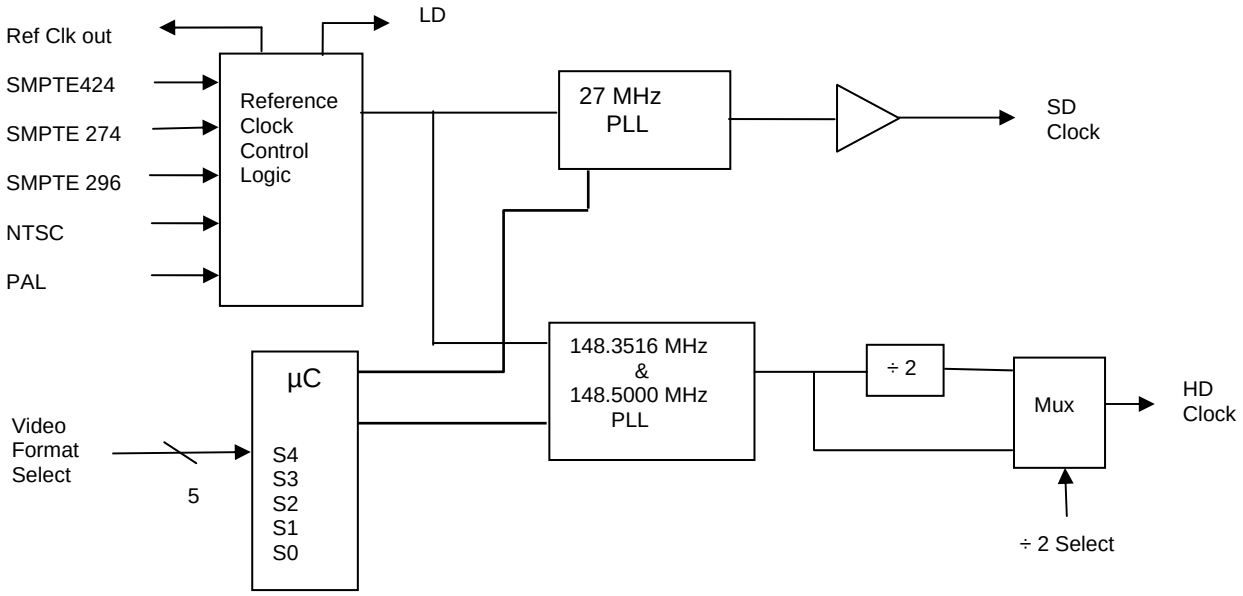
RoHS Status

RoHS 6/6

Features
- Low Jitter HD and SD Clock Sources
- Completely Integrated Timing Solution

Applications
- SMPTE 274 Systems
- SMPTE 296 Systems
- SMPTE 424 3Gb/s re-clocking
- NTSC
- PAL

Description:
The VFCG-HD-1 is a fully integrated video clock generator which provides synchronous High Definition (HD) and Standard Definition (SD) output clocks for the various scanning formats. The device synchronizes to the standard input reference clock required by SMPTE274, SMPTE296, NTSC or PAL systems. A 5-bit address is used to synchronize the generator to the appropriate input reference clock. A dedicated control signal divides the maximum HD clock rate by 2 in order to support HD clock rates of 74.25 MHz and 74.1758 MHz.



Block Diagram

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Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Break Down Voltage	Vcc		-0.5		4.6	V	
Storage Temperature	Ts		-55		+105°	°C	

Operating Specification

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Output Frequency	HD-out	÷2 sel = "0" ÷2 sel = "1"	148.3516 74.17582		148.500 74.250	MHz	See Table 1
	SD_out			27.00		MHz	See Table 1
Input Frequency	Fin		15.625		10,000.0	KHz	See Table 1
Input Level	Vin		2.2		3.3	V p-p	Falling edge triggered
Output Level Logic "1"	Voh	IOH = 8 mA	Vcc-.6		Vcc	V	LVCMOS
Output Level Logic "0"	Vol	IOL = 8 mA	0.0		.3	V	LVCMOS
Phase Jitter				1	2	ps(rms)	
Peak to Peak Jitter				7	10	ps	
Input Tracking Range			± 50			ppm	
Modulation BW	MBW		10			Hz	
Duty Cycle		@ 50%	45	50	55	%	
Rise / Fall Time	Tr/Tf	20% to 80%		.6		ns	
Initial Lock time					4	s	
Supply Voltage	Vcc		3.15	3.30	3.45	V	
Input Current	Icc			60	80	mA	
Operating Temperature Range	Ta		-40°		+85°	°C	
Lock Detect	LD	Output HIGH (> 2.5 V) : In Lock; Output LOW (< .5V): Out of Lock					LVCMOS
÷ 2 Sel input	÷ 2 Sel	Logic "0" : HD_out = 148 MHz; Logic "1" or floating HD_out = 74 MHz					LVCMOS

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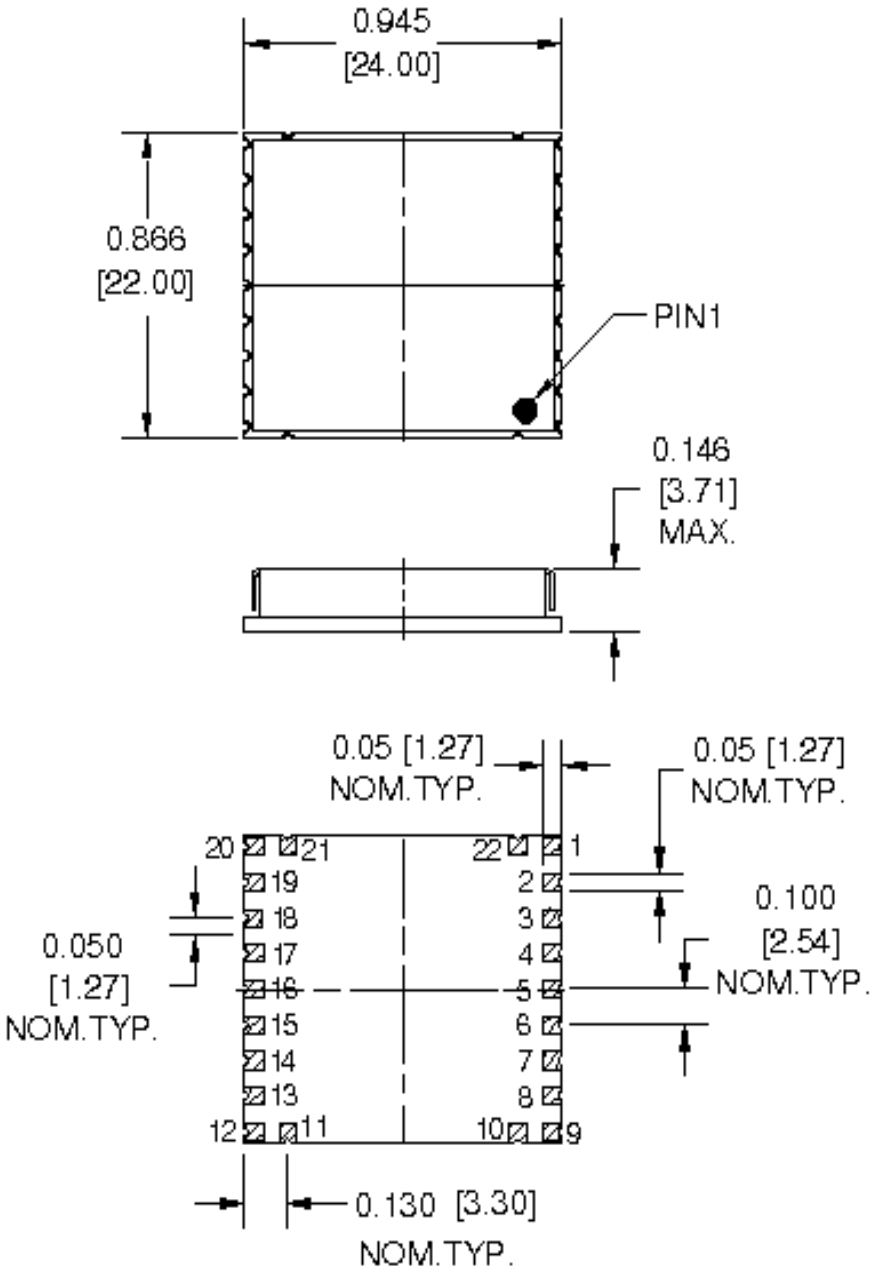
Table 1

I/O Select (HEX)	Input Ref (KHz)	HD output (MHz)	SD/HD ratio	SD output (MHz)
00	67.5	148.50	4/22	27
01	56.25	148.50	4/22	27
02	33.75	148.50	4/22	27
03	28.125	148.50	4/22	27
04	27	148.50	4/22	27
05	45	148.50	4/22	27
06	37.5	148.50	4/22	27
07	22.5	148.50	4/22	27
08	18.75	148.50	4/22	27
09	18	148.50	4/22	27
0A	67.43257	148.3516484	91/500	27
0B	33.71628	148.3516484	91/500	27
0C	26.97303	148.3516484	91/500	27
0D	44.95504	148.3516484	91/500	27
0E	22.47752	148.3516484	91/500	27
0F	17.98202	148.3516484	91/500	27
10	15.73427	148.50	4/22	27
11	15.73427	148.3516484	91/500	27
12	15.625	148.50	4/22	27
13	15.625	148.3516484	91/500	27
14	10,000.0	148.50		27
15	10,000.0	148.3516484		27
16	74,175.8242	148.50		27
17	74,250.00	148.3516484		27

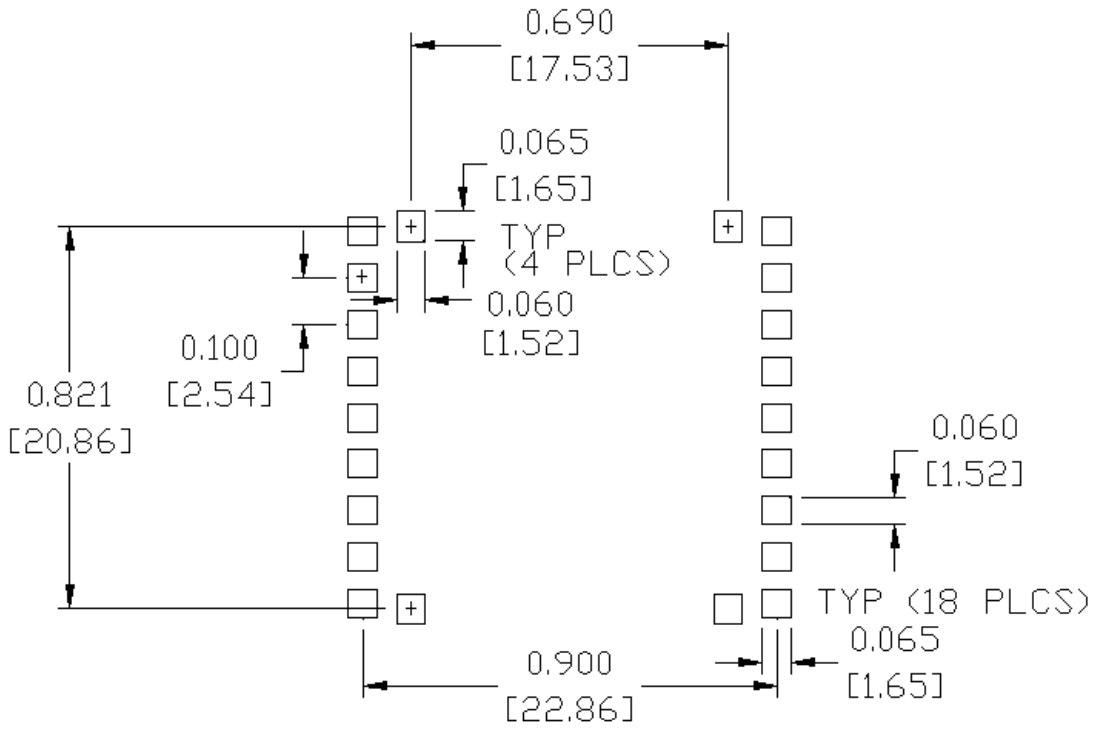
Pin Assignments

Pin #	Symbol	Description	Notes
1	Fref-out	Reference Clock Output	Inverts Fref-in
2	Fref-in	Reference Clock Input	
3	S0	I/O Select (LSB)	
4	Vccp	+3.3V Power Supply	Connect to pin #5 and add .1 uF Cap
5	Vcc	+3.3V Power Supply	Connect to pin #4 and add .1 uF Cap
6	S1	I/O Select	
7	S2	I/O Select	
8	S4	I/O Select (MSB)	
9	S3	I/O Select	
10	Gnd	Ground	
11	Gnd	Ground	
12	TP2	Test Pt	Do not Connect
13	HD_out	High Definition Clk Outout	
14	÷ 2 Sel	Divide by 2 Select	Divides the HD_out clk by 2
15	Vcc	+3.3V Power Supply	
16	SD_out	Standard Definition Clk Output	
17	Gnd	Ground	
18	LD	Lock Detect	
19	Gnd	Ground	
20	TP1	Test Pt	Do not Connect
21	Gnd	Ground	
22	Gnd	Ground	

Mechanical Outline



Recommended Pad Layout



RECOMMENDED PAD LAYOUT