FEATURES

• Standard 7x5mm Surface Mount Footprint
• HCMOS/TTL Compatible
• Fundamental and 3rd Overtone Crystals
• Frequency Range 1 – 125 MHz
• Frequency Stability, ±50 ppm Standard
  (±25 ppm and ±20 ppm available)
• +2.5Vdc Operation
• Operating Temperature to –40°C to +85°C
• Output Enable Standard
• Tape & Reel Packaging
• RoHS/ Green Compliant

DESCRIPTION

The CB2V5 is a ceramic packaged Clock oscillator offering reduced size and enhanced stability. The small size means it is perfect for any application. The enhanced stability means it is the perfect choice for today’s communications applications that require tight frequency control.

ORDERING INFORMATION

Example Part Number: CB2V53C032M7680
### ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Absolute Maximums</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Supply Voltage</td>
<td>VCC</td>
<td>-</td>
<td>-0.5</td>
<td>-</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>TSTG</td>
<td>-</td>
<td>-55</td>
<td>-</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Frequency Range</td>
<td>fO</td>
<td>-</td>
<td>1.0</td>
<td>-</td>
<td>125</td>
<td>MHz</td>
</tr>
<tr>
<td>Frequency Stability</td>
<td>Δf/fO</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>20,25,50 or 100</td>
<td>± ppm</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Commercial</td>
<td>T,A</td>
<td>-</td>
<td>-20</td>
<td>25</td>
<td>70</td>
<td>85</td>
</tr>
<tr>
<td>Industrial</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>VCC</td>
<td>± 10 %</td>
<td>2.25</td>
<td>2.50</td>
<td>2.75</td>
<td>V</td>
</tr>
<tr>
<td>Supply Current</td>
<td>ICC</td>
<td>1.0 MHz to 20 MHz</td>
<td>-</td>
<td>-</td>
<td>7</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20.1 MHz to 50 MHz</td>
<td>Cc=15pF</td>
<td>-</td>
<td>15</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>50.1 MHz to 125 MHz</td>
<td>Cc=15pF</td>
<td>-</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td>Output Load</td>
<td>CL</td>
<td>1.0 MHz to 50 MHz</td>
<td>-</td>
<td>-</td>
<td>30</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>50.1 MHz to 125 MHz</td>
<td>-</td>
<td>-</td>
<td>15</td>
<td>pF</td>
</tr>
<tr>
<td>Output Voltage Levels</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic '1' Level</td>
<td>VOH</td>
<td>-</td>
<td>90%VCC</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Logic '0' Level</td>
<td>VIL</td>
<td>-</td>
<td>10%VCC</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Output Current</td>
<td>IC1</td>
<td>VOH = 90%VCC</td>
<td>-</td>
<td>-</td>
<td>-4</td>
<td>mA</td>
</tr>
<tr>
<td>Logic '1' Level</td>
<td>IC1</td>
<td>VCC = 10%VCC</td>
<td>-</td>
<td>-</td>
<td>+4</td>
<td>mA</td>
</tr>
<tr>
<td>Logic '0' Level</td>
<td>IC1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>%</td>
</tr>
<tr>
<td>Output Duty Cycle</td>
<td>SYM</td>
<td>@ 50% Level</td>
<td>45</td>
<td>-</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>Rise and Fall Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T.R, T.F</td>
<td></td>
<td>@ 10% - 90% Levels</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.0 MHz to 20 MHz</td>
<td>Cc=15pF</td>
<td>-</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20.1 MHz to 50 MHz</td>
<td>Cc=15pF</td>
<td>-</td>
<td>4</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>50.1 MHz to 125 MHz</td>
<td>Cc=15pF</td>
<td>-</td>
<td>3</td>
<td>ns</td>
</tr>
<tr>
<td>Start Up Time</td>
<td>TS</td>
<td>Application of VCC</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>ms</td>
</tr>
<tr>
<td>Enable Function</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Enable Input Voltage</td>
<td>VIL</td>
<td>Pin Logic '1', Output Enabled</td>
<td>1.75</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Disable Input Voltage</td>
<td>VIL</td>
<td>Pin Logic '0', Output Disabled</td>
<td>-</td>
<td>-</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>Standby Current</td>
<td>IST</td>
<td>VIL = 0.58V, Oscillator Stops</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td>Output Enable Time</td>
<td>TOPLZ</td>
<td>VIL = 1.58V</td>
<td>-</td>
<td>-</td>
<td>8</td>
<td>ms</td>
</tr>
<tr>
<td>Phase Jitter</td>
<td>tJms</td>
<td>Bandwidth 12 kHz - 20 MHz</td>
<td>-</td>
<td>&lt; 1</td>
<td>-</td>
<td>ps RMS</td>
</tr>
</tbody>
</table>

**Notes:**

1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and first year aging at an average operating temperature of +40 °C.
Model CB2V5
7x5mm Low Cost
HCMOS/TTL Clock Oscillator

CMOS/TTL OUTPUT WAVEFORM

DUTY CYCLE = UT x 100 (%)

90%, 80%, 2.6V
50%, 1.5V
10%, 20%, 0.5V

TEST CIRCUIT, CMOS LOAD

Enable Input

D.U.T. PIN ASSIGNMENTS

<table>
<thead>
<tr>
<th>PIN</th>
<th>SYMBOL</th>
<th>DESCRIPTION</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>EOH</td>
<td>Enable Input</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Circuit &amp; Package Ground</td>
</tr>
<tr>
<td>3</td>
<td>Output</td>
<td>RF Output</td>
</tr>
<tr>
<td>4</td>
<td>VCC</td>
<td>Supply Voltage</td>
</tr>
</tbody>
</table>

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING

CTS ** - 2V5

XXXMXXXX

YYWW

PIN 1 IDENTIFIER

(1.2) 0.047

(3.7) 0.146

(1.4) 0.055

(1.8) 0.071 MAX

SUGGESTED SOLDER PAD GEOMETRY

C_BYPASS

0.079 [2.00]

0.165 [4.20]

0.200 [5.08]

C_BYPASS should be ≥ 0.01 uF.

SUGGESTED REFLOW PROFILE

Maximum 260°C, 10 seconds

Typical 245°C

130°C

Enable Input

Cl.

Including probe capacitance.

MARKING INFORMATION

1. ** - Manufacturing Site Code.
2. XXXMXXXX - Frequency marked with 4 significant digits after the 'M'.
3. YYWW – Date code, YY – year, WW – week.

NOTES

1. Termination pads (e4), barrier-plating is nickel (Ni) with gold (Au) flash plate.
2. Reflow conditions per JEDEC J-STD-020.

ENABLE TRUTH TABLE

<table>
<thead>
<tr>
<th>PIN 1</th>
<th>PIN 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic '1'</td>
<td>Output</td>
</tr>
<tr>
<td>Open</td>
<td>Output</td>
</tr>
<tr>
<td>Logic '0'</td>
<td>High Imp.</td>
</tr>
</tbody>
</table>

DUTY CYCLE = UT x 100 (%)

VGH

VOL

POUT

OUP

Tr

Tf

UPTIME (t)

Power Supply

+ -

+ -

VM

mA

0.01uF

D.U.T.

43

12

34

C BYPASS

Enable Input

CMOS/TTL OUTPUT WAVEFORM

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90%, 80%, 2.6V
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10%, 20%, 0.5V

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Enable Input

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7x5mm Low Cost
HCMOS/TTL Clock Oscillator

TAPE AND REEL INFORMATION

DIMENSIONS IN MILLIMETERS

Device quantity is 1,000 pieces per 180mm reel.

ENVIRONMENTAL SPECIFICATIONS

Temperature Cycle: 400 cycles from –55°C to +125°C, 10 minute dwell at each temperature, 1 minute transfer time between temperatures.

Mechanical Shock: 1,500g’s, 0.5mS duration, ½ sinewave, 3 shocks each direction along 3 mutually perpendicular planes (18 total shocks).

Sinusoidal Vibration: 0.06 inches double amplitude, 10 to 55 Hz and 20g’s, 55 to 2,000 Hz, 3 cycles each in 3 mutually perpendicular planes (9 times total).

Gross Leak: No leak shall appear while immersed in an FC40 or equivalent liquid at +125°C for 20 seconds.

Fine Leak: Mass spectrometer leak rates less than 2x10⁻⁸ ATM cc/sec air equivalent.

Resistance to Solder Heat: Product must survive 3 reflows of +260°C peak, 10 seconds maximum.

High Temperature Operating Bias: 2,000 hours at +125°C, maximum bias, disregarding frequency shift.

Frequency Aging: 1,000 hours at +85°C, full bias, less than ±5 ppm shift.

Moisture Sensitivity Level: Level 1 per JEDEC J-STD-020.

QUALITY AND RELIABILITY

Quality systems meet or exceed the requirements of ISO 9000:2000 standards.